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Configuration for a Grounded Lossy Impedance Simulator Employing CC-CFAs and Grounded Passive Elements

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Abstract: This article presents a configuration that can simulate both a resistor in series with a frequency-dependent negative-resistance (R-D) and a resistor in series with a capacitor (R-C), with a different selection of passive elements. The proposed circuit employs only two current-controlled-current-feedback- amplifiers (CC-CFAs) and grounded passive elements. This configuration does not require passive element matching, and the simulated equivalent element values can be tuned electronically by applying a biasing current to the CC-CFAs. To demonstrate the application of the proposed grounded series R-D impedance simulator, it is applied to a second-order notch filter and a fifth-order elliptic low-pass filter, whereas the series R-C impedance simulator is applied to a second-order resonance circuit to find the band-pass response of the input current. Our theoretical analysis is confirmed by the results of a PSPICE simulation.

Keywords: Frequency-dependent negative-resistance (FDNR), Current controlled-CFA (CC-CFA), Capacitance multiplier, Elliptic filter.

1 Introduction

In analogue signal processing/generation circuits, large-valued capacitors are often very useful for the design of low-frequency circuits. Due to the limitations on the fabrication of large-valued capacitors in integrated circuits (ICs), a capacitor multiplier circuit is the preferred choice of researchers. The function of the capacitor multiplier circuit is to increase the value of the capacitance, and it is mostly applied in low-frequency filters and long-duration timing circuits. These capacitance multipliers can be designed using active R-C circuits, which are also useful for sinusoidal oscillators and active R-C filters. Numerous configurations that can function as a capacitance multiplier have been reported in

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the literature [1 – 17]. There are several methods for realising capacitance multipliers using an operational transconductance amplifier (OTA) [2, 3], electronically tunable floating general impedance inverter (EGII) [4], operational transresistance amplifier (OTRA) [5], current controlled current conveyor (CCCII) [6], current conveyor (CC) [7], differential voltage current conveyor (DVCC) [8], second generation current conveyor (CCII) [9], second generation inverting current conveyor (ICCII) [10], voltage differencing inverting buffered amplifier (VDIBA) [11], voltage differencing buffered amplifier (VDBA) [12], or current feedback operational amplifier (CFOA) [13 – 17]. We note that the schemes reported in [2, 3, 5, 9, 11, 13] need at least three passive components for their realisation, and that the circuit presented in [2 – 8, 13] cannot be tuned electronically.

In any passive ladder filter, there will be a combination of *R-L-C* components; of these, inductors are particularly problematic components due to their larger size and weight. To replace passive inductors, researchers have devised many options involving grounded simulated inductors, but when it comes to floating inductors, the designs are a little more complicated, and they employ a large number of active and passive elements. Bruton [18] proposed an inductor transformation technique and a new element called a frequency-dependent negative resistor (FDNR) or *D*-component, which has a purely real negative resistance $-1/\omega^2 C = -1/\omega^2 D$ meaning that the gain declines in magnitude at a rate of −40 dB per decade. Bruton [18] stated that "if all the impedances of a passive ladder filter are divided by s, the transfer function is not changed." The transformation of passive elements is as follows: resistors are transformed to capacitors as $1/R \to C$, inductors into resistors as $L \to R$, and capacitors into FDNRs as $C \to D$. Several works addressing the realisation of FDNRs with dissimilar types of active building blocks are available in the literature [18 – 27].

In this article, we present a generalised circuit consisting of two CC-CFAs and two grounded impedances. This can act as a grounded series R-D simulator when we choose both impedances as capacitors, and a grounded series R-C simulator when one is a resistor and the other is a capacitor. The proposed circuit exhibits superior characteristics to the existing ones in terms of the number of active and passive elements and its functionality. Also, it does not require matching of the components. As an application, an R-D simulator is used in a fifth-order elliptic low-pass filter. It has advantages over other simulators, as this FDNR is in series with a resistor, which reduces the number of resistor requirements. The proposed R-D simulator is also used to realise a second-order notch-filter. Similarly, an R-C impedance simulator circuit is employed to realise a second-order band-pass filter as an example of an application. The outcomes of the simulation are found to confirm the theory.

2 Proposed Configuration Circuit

The symbol of CC-CFA and an equivalent circuit are shown in Figs. 1a and 1b respectively. Its input and output terminal characteristics can be depicted by the matrix equation (1):

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \\ i_w \end{bmatrix}, \tag{1}$$

where

$$R_x = \frac{V_T}{2I_B}. \tag{2}$$

The CC-CFA was presented in 2008 by Siripruchyanun et al. [28]. Its properties are comparable to those of a conventional CFA, except that a CC-CFA has a finite input resistance R_x at the X input terminal and the magnitude of the parasitic resistance R_x can be controlled by the dc bias current I_B and the thermal voltage V_T.

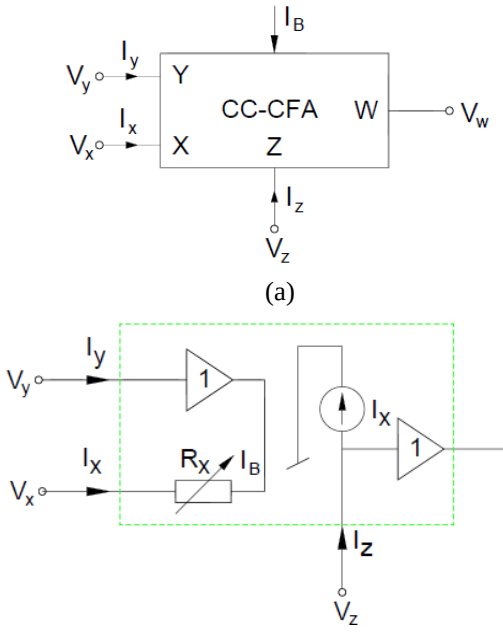


Fig. 1 – (a) *Diagram of the CC-CFA symbol;* (b) *Equivalent circuit.*

The proposed grounded impedance simulator configuration, presented in Fig. 2, employs two CC-CFAs and two grounded passive elements. The input impedance can be expressed as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = R_{x1} + \frac{Z_1 Z_2}{R_{x2}}. \tag{3}$$

Based on (3), several different input impedance values can be obtained as follows.

Case I: If we choose $Z_1 = \frac{1}{sC_1}$ and $Z_2 = \frac{1}{sC_2}$, (3) can be rewritten as

$$Z_{in} = R_{x1} + \frac{1}{s^2 C_1 C_2 R_{x2}} = R_{eq} + \frac{1}{s^2 D_{eq}}. \tag{4}$$

Equation (4) states that the circuit in Fig. 2 can be realised as a lossy FDNR (i.e., a grounded resistance in series with an FDNR), where

$$R_{eq} = R_{x1}, D_{eq} = C_1 C_2 R_{x2} = C_1 C_2 \frac{V_T}{2I_{B2}}. \tag{5}$$

Case II: If we select $Z_1 = \frac{1}{sC_1}$ and $Z_2 = R_2$, (3) is reduced to

$$Z_{in} = R_{x1} + \frac{R_2}{sC_1 R_{x2}} = R_{eq} + \frac{1}{sC_{eq}}. \tag{6}$$

Equation (6) states that the circuit in Fig. 2 can be realised as a lossy capacitance multiplier (i.e. a grounded resistance in series with a capacitor), where

$$R_{eq} = R_{x1}, \quad C_{eq} = \frac{R_{x2}}{R_2} C_1 = \frac{C_1}{R_2} \frac{V_T}{2I_{B2}}. \tag{7}$$

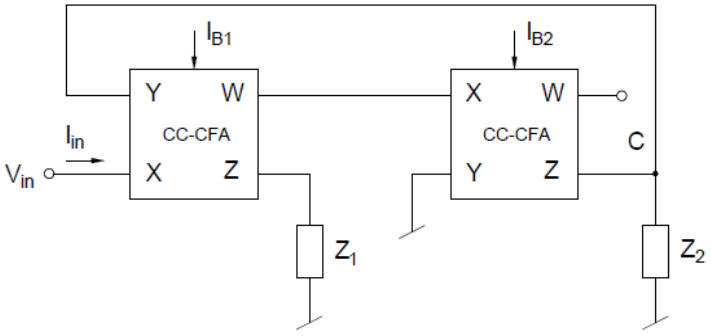


Fig. 2 – *Proposed lossy grounded impedance simulator.*

2.1 Non-ideality and sensitivity analysis

An equivalent circuit model for the non-ideal CC-CFA is shown in Fig. 3. Here, R_y, R_z, R_w, and C_y, C_z are the parasitic resistances and capacitances at the ports Y, Z, and W respectively. The terminal characteristics of a non-ideal CC-CFA can be represented in the *s*-domain as:

$$v_x = \beta v_y + R_x i_x, \tag{8}$$

$$i_y = \left(sC_y + \frac{1}{R_y} \right) v_y, \tag{9}$$

$$i_z = \alpha i_x + \left(sC_z + \frac{1}{R_z} \right) v_z, \tag{10}$$

$$v_w = \gamma v_z + R_w i_w. \tag{11}$$

To evaluate the effect of parasitic elements on the input impedance of the proposed circuit, we set the values of α, β and γ to unity for simplicity. The input impedance of the circuit in Fig. 2 can be calculated as follows:

$$\begin{aligned} Z_{in} = \frac{V_{in}}{I_{in}} = R_{x1} + R_{z1}R_{z2}R_{y1}Z_1Z_2 \Big/ \{ R_{x2}(R_{z1} + Z_1 + sC_{z1}R_{z1}Z_1) \cdot \\ \cdot (R_{z2}R_{y1} + Z_2R_{y1} + Z_2R_{z2} + sZ_2R_{z2}R_{y1}(C_{z2} + C_{y1})) \}, \end{aligned} \tag{12}$$

$$R_{z1} \gg Z_1 + sC_{z1}R_{z1}Z_1, \tag{13}$$

$$R_{z2}R_{y1} \gg Z_2R_{y1} + Z_2R_{z2} + sZ_2R_{z2}R_{y1}(C_{z2} + C_{y1}), \tag{14}$$

where R_{z1}, R_{z2}, C_{z1}, and C_{z2} are parasitic elements at the z-terminal, and R_{y1} and C_{y1} are the parasitic elements at the y-terminal, as shown in Fig. 3, for both of the CC-CFAs in Fig. 2.

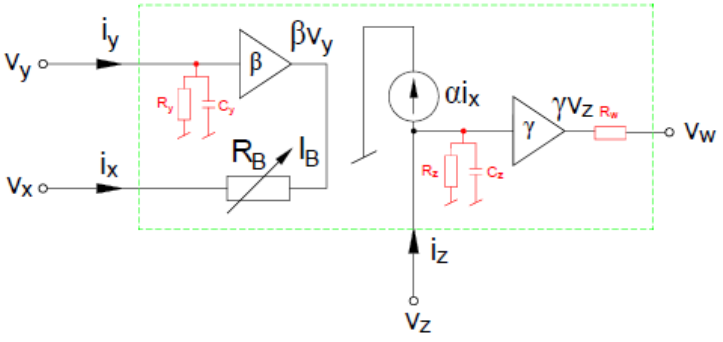


Fig. 3 – *Non-ideal equivalent circuit for a CC-CFA.*

The overall effect of the parasitic elements on the input impedance of the proposed circuit is negligible. In the case of an FDNR, Z_1 and Z_2 are the capacitive impedance, and the last term in (13) and (14) becomes a resistive term.

To evaluate the effects of non-ideal current and voltage gain on the proposed circuit in Fig. 2, we consider the characteristics of the CC-CFA as presented in [28]. We also presume that no offset voltage and current occur in the CC-CFA, and that v_x, i_z and v_w for the CC-CFA can be expressed as:

$$\begin{aligned} i_z &= \alpha i_x, \\ v_x &= \beta v_y + i_x R_x, \\ v_w &= \gamma v_z. \end{aligned} \tag{15}$$

Here, α, β and γ are transferred error values, which may deviate from ideal conditions. When we include the effects of α, β and γ on the configuration in Fig. 2, the input impedance is revised as follows:

$$Z_{in} = R_{x1} + \frac{\alpha_1\alpha_2\beta_1\gamma_2 Z_1 Z_2}{R_{x2}}. \tag{16}$$

From (16) we see that for the non-ideal case, the circuit in Fig. 2 simulates a grounded R-D simulator with values

$$R_{eq} = R_{x1}, \quad D_{eq} = \frac{C_1 C_2 R_{X2}}{\alpha_1\alpha_2\beta_1\gamma_2}. \tag{17}$$

In the same way, the values of the grounded R-C simulator circuit, presented in Fig. 2, are expressed as:

$$R_{eq} = R_{x1}, \quad C_{eq} = \frac{C_1 R_{x2}}{\alpha_1\alpha_2\beta_1\gamma_2 R_2}. \tag{18}$$

If these error factors tend to unity, the change in the R-D and R-C values in (17) and (18) can be ignored. α, β and γ arise from the intrinsic resistances and stray capacitances in the CC-CFA.

The sensitivities of the active and passive elements in (17) are shown below, and it can be seen that these are very low.

$$\begin{aligned} s_{R_{x1}}^{R_{eq}} &= 1, \\ s_{C_1}^{D_{eq}} = s_{C_2}^{D_{eq}} &= s_{R_{x2}}^{D_{eq}} = 1, \\ s_{\alpha_1}^{D_{eq}} = s_{\alpha_2}^{D_{eq}} &= s_{\beta_1}^{D_{eq}} = s_{\gamma_2}^{D_{eq}} = -1. \end{aligned} \tag{19}$$

The sensitivities of the active and passive elements from (18) are shown below. Again, it can be seen that these are very low.

$$s_{R_{x1}}^{R_{eq}} = 1,$$
$$s_{C_1}^{C_{eq}} = s_{R_{x2}}^{C_{eq}} = 1, \tag{20}$$
$$s_{R_2}^{C_{eq}} = s_{\alpha_1}^{C_{eq}} = s_{\alpha_2}^{C_{eq}} = s_{\beta_1}^{C_{eq}} = s_{\gamma_2}^{C_{eq}} = -1.$$

3 Simulation and Experimental Results with Example Applications

Figs. 5b, 9b and 11 illustrate some applications of the proposed grounded lossy impedance simulator, and the results were verified with a PSPICE simulation model. The internal structure of a CC-CFA based on mixed-mode translinear cells can be made using a BJT, CMOS or BiCMOS technologies. For the condition $i_x(t) << 2I_B$, the magnitude of the parasitic resistance (R_x) at the X-input terminal using BJT or BiCMOS implementation can be expressed as follows:

$$R_x = \frac{kT/q}{2I_B} = \frac{V_T}{2I_B}. \tag{21}$$

The above equation shows that the magnitude of R_x can be changed by altering the dc bias current I_B.

The circuit topology for the CC-CFA implementation with a BJT can easily be transformed into CMOS technology by simply replacing the PNP and NPN transistors with PMOS and NMOS transistors, respectively. There are two operating conditions that may occur: the MOS transistors can either operate in the weak inversion region, or the strong inversion region. If the MOS transistors are operating in a weak inversion (or subthreshold) region with a small bias current, then the current equation is [29]:

$$I_D = \frac{W}{L} I_{D0}\, \mathrm{e}^{\frac{qV_{GS}}{nkT}} \left(1 - \mathrm{e}^{-\frac{qV_{DS}}{kT}}\right), \tag{22}$$

where the value of *n* is typically 1.2 – 1.5 and I_{D0} is the drain current at $V_{DS} = 0\,\mathrm{V}$ for $W/L = 1.$

If we neglect the term $\mathrm{e}^{-qV_{DS}/kT}$, then R_x can be obtained using (21). If the value of the dc bias current I_B is high enough, then the MOS transistors are operating in a strong inversion (or saturation) region, and R_x can be obtained as follows:

$$R_x = \frac{1}{g_{mQ2} + g_{mQ4}}, \tag{23}$$

where

$g_{mQi} = \sqrt{2\beta_i I_B}$, $(i = 2,4)$, and g_{mQ2} and g_{mQ4} are the transconductances of the translinear cell MOS transistors. Thus, R_x can still be adjusted via I_B if CMOS CC-CFAs are used. The R_x of a CMOS CC-CFA has a nonlinear relationship (square root) to I_B, and also depends on the process parameters, as shown in (22) and (23). In contrast, a BJT or BiCMOS implementation has a linear relationship, as shown in (1), which provides a wide range of electronic tunability. We therefore used a BiCMOS realisation of a CC-CFA [28] in the test circuits, as shown in Fig. 4. The parameters of PR200N (PNP) and NR200N (NPN) bipolar transistors of an ALA400 transistor array from AT&T [30] were employed in the circuit, while 0.35 μm TSMC CMOS technology [31] was replicated in the PMOS and NMOS transistors, and the operating voltage supply was ± 1.5V. The aspect ratios for the MOS transistors are given in **Table 1**.

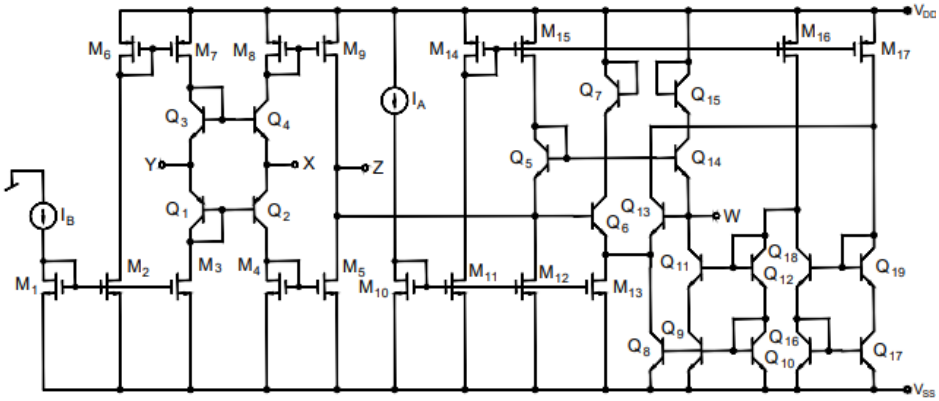


Fig. 4 – *BiCMOS current-controlled current feedback amplifier.*

Table 1
Aspect ratios of MOS transistors.

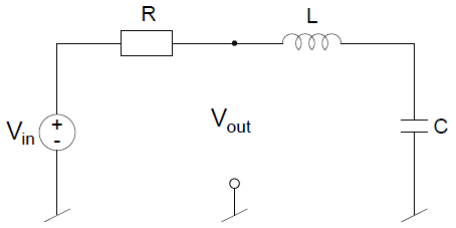
NMOS/PMOS transistors	W[μm]/L[μm]
M_1	7.5/0.5
M_2	8.5/0.5
M_3	9/0.5
M_4-M_5, M_{14}-M_{15}	5/0.5
M_6-M_9	15/0.5
M_{10}-M_{13}	4/0.5
M_{16}-M_{17}	10/0.5

3.1 Examples of grounded R-D simulators

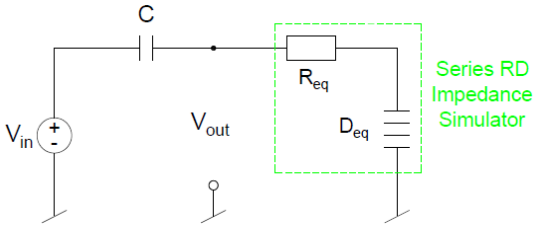
3.1.1 Voltage-mode R-L-C second-order notch filter

The voltage-mode second-order notch filter shown in Fig. 5a was implemented using the proposed grounded series R-D simulator in Fig. 2. By applying Bruton's [18] transformation technique to Fig. 5a, the realisation of FDNR employed filter is shown in Fig. 5b, for which the transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{s^2 + \dfrac{1}{R_{eq}D_{eq}}}{s^2 + \dfrac{s}{R_{eq}C} + \dfrac{1}{R_{eq}D_{eq}}}. \tag{24}$$



(a)



(b)

Fig. 5 – (a) *Passive RLC circuit for transformation;*
(b) *Simple prototype CRD used to verify the theory.*

The circuit in Fig. 5b was simulated with values for the passive components as follows: $C = 0.513\,\text{nF}$; for D_{eq}: $C_1 = C_2 = 0.513\,\text{nF}$, $R_{x1} = 10\,\text{k}\Omega$, $R_{x2} = 10\,\text{k}\Omega$, leading to values of $R_{eq} = 10\,\text{k}\Omega$, $D_{eq} = 2,631\,\text{pFs}$. This resulted in a centre frequency of $f_c = 32\,\text{kHz}$ and a quality factor of $Q_o = 1$. The simulated response of the voltage-mode filter is shown in Fig. 6, where the electronic adjustment of f_c for the notch filter was achieved by changing the current I_{B1}.

To verify our theoretical results, we used a commercially available CFOA/CFA AD844AN IC. For the parasitic resistance R_x, a resistor of 10 kΩ

was connected at port X to construct the circuit in Fig. 2. The R-L-C notch filter obtained using an FDNR was experimentally tested with a supply voltage of ±12V. Fig. 7 shows the experimental setup for the R-L-C notch filter in Fig. 5b, which was prototyped with measured values of the passive components of $R = 10\,\mathrm{k}\Omega$ and $C = 610\,\mathrm{pF}$. The calculated centre frequency was 25.119 kHz, where the resistor value was fixed. The experimental and theoretical results are shown in Fig. 8, and the experimental centre frequency was found to be 25.5 kHz, which agreed well with the theoretical value.

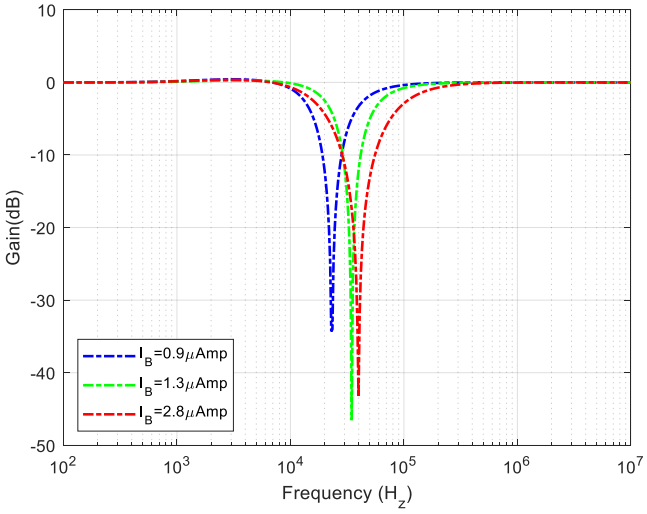


Fig. 6 – *Simulated frequency response for the voltage-mode R-L-C second-order notch filter in Fig. 5b.*

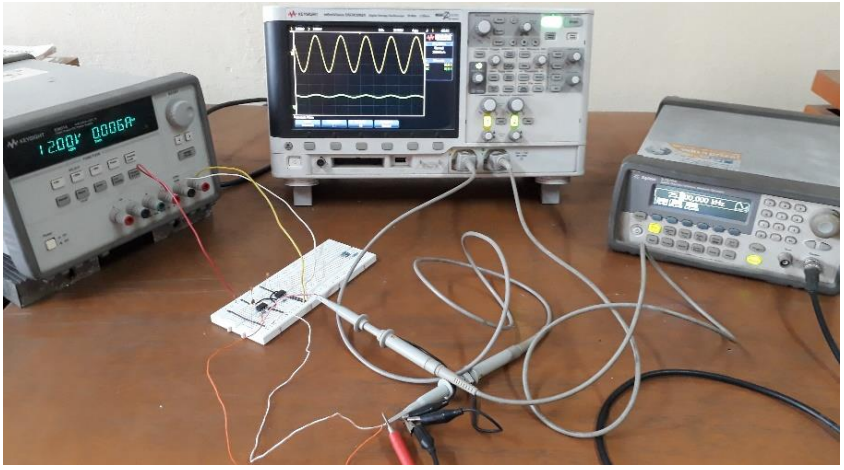


Fig. 7 – *Experimental setup.*

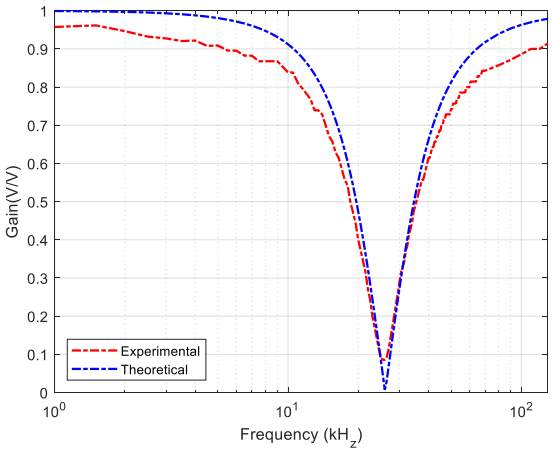


Fig. 8 – *Experimental and theoretical frequency responses of the voltage-mode R-L-C second-order notch filter in Fig. 5b.*

3.1.2 Voltage-mode R-L-C low-pass fifth-order elliptic filter

The functionality of the proposed grounded series R-D impedance simulator circuit was verified using a R-L-C low-pass fifth-order elliptic filter, as shown in Fig. 9. The R-L-C ladder network can be converted to an equivalent FDNR-based network denoted as C-R-D by scaling the impedance parameters, as suggested by Bruton [18], and this is shown in Fig. 9b.

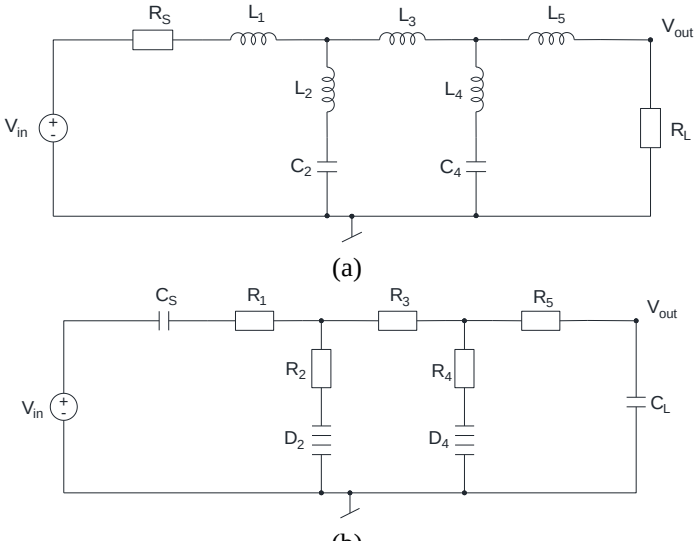


Fig. 9 – *Transformation of a low-pass elliptic R-L-C ladder filter using Bruton's [18] technique:* (a) *Doubly terminated R-L-C network;* (b) *Transformed C-R-D network.*

For the circuit in Fig. 9a, the values of the normalised passive elements for a cut-off frequency of 1 Hz are: $R_S = R_L = 1\,\mathrm{k}\Omega$, $L_1 = 1.977\,\mathrm{H}$, $L_2 = 0.188\,\mathrm{H}$, $L_3 = 2.492\,\mathrm{H}$, $L_4 = 0.520\,\mathrm{H}$, $L_5 = 1.719\,\mathrm{H}$, $C_2 = 0.977\,\mathrm{F}$ and $C_4 = 0.794\,\mathrm{F}$. For a cut-off frequency of 40 kHz, the values of the *C*, *R* and *D* elements in Fig. 9b are:

$$C_S = C_L = 2\,\mathrm{nF}, \quad R_1 = 3.934\,\mathrm{k}\Omega, \quad R_3 = 4.959\,\mathrm{k}\Omega, \quad R_5 = 3.42\,\mathrm{k}\Omega,$$

$$R_{eq2} = R_{x12} = 0.374\,\mathrm{k}\Omega, \quad D_2 = C_{12}C_{22}R_{x22},$$

where

$$C_{12} = 1.95\,\mathrm{nF}, \quad C_{22} = 2\,\mathrm{nF}, \quad R_{x22} = 2\,\mathrm{k}\Omega,$$

$$R_{eq4} = R_{x14} = 1.0348\,\mathrm{k}\Omega, \quad D_4 = C_{14}C_{24}R_{x24},$$

where

$$C_{14} = 1.588\,\mathrm{nF}, \quad C_{24} = 2\,\mathrm{nF}, \quad R_{x24} = 2\,\mathrm{k}\Omega.$$

Fig. 10 shows the results of a PSPICE simulation of the frequency response of the circuit in Fig. 9b.

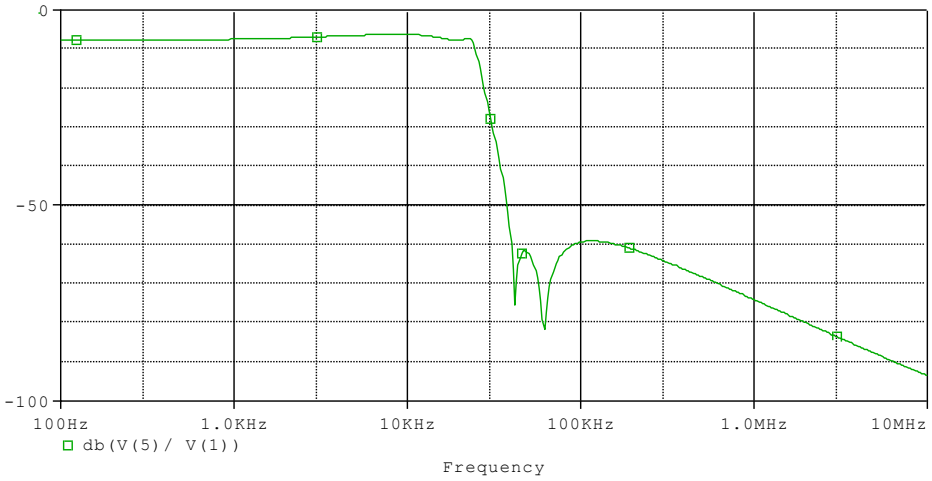


Fig. 10 – *Frequency response of the voltage-mode fifth-order elliptic low-pass filter in Fig. 9b.*

3.2 Grounded R-C simulator

To validate our results for the grounded series R-C impedance circuit, the active R-L-C circuit in Fig. 11 was used. Here, the passive floating inductor is replaced by an active lossless floating inductor [32]. The derived input current for the circuit in Fig. 11 is expressed as

$$I_{in} = V_{in} \frac{s\dfrac{1}{L}}{s^2 + s\dfrac{R_{eq}}{L} + \dfrac{1}{LC_{eq}}}. \tag{25}$$

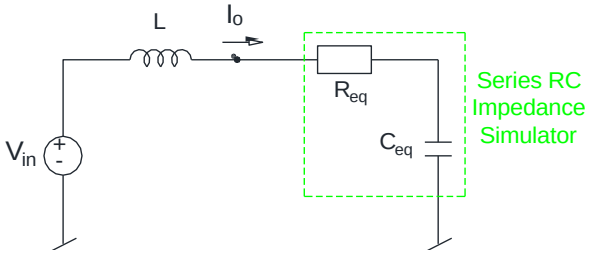


Fig. 11 – *An active R-L-C second-order resonance circuit.*

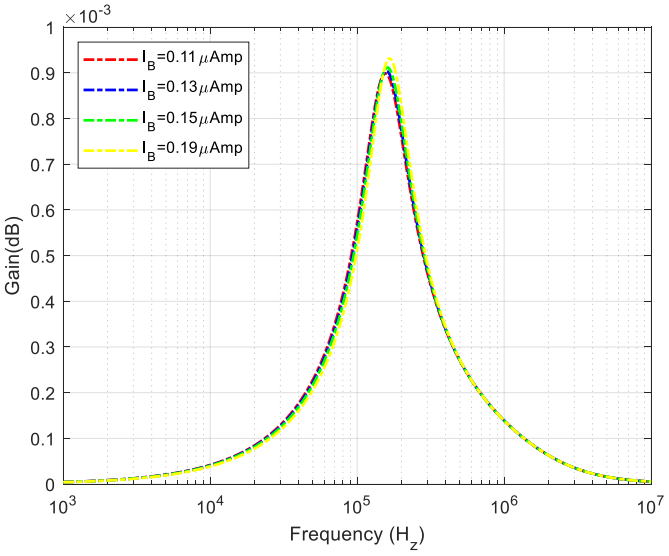


Fig. 12 – *Simulated frequency response for the current in the R-L-C circuit shown in Fig. 11.*

To realise the circuit in Fig. 11 for centre frequency $f_c = 159\,\text{kHz}$, for $L = L_{eq} = 1\ \text{mH}$ select the circuit component values as $C = 0.1\ \text{nF}$, $R_{x1} = 0.5\ \text{k}\Omega$, $R_{x2} = 0.5\ \text{k}\Omega$ and $R_{x3} = 10\ \text{k}\Omega$, and for $R = 1\ \text{k}\Omega$ and $C = 1\ \text{nF}$ choose the R-C simulator circuit component values as $C_1 = 1\ \text{nF}$, $R_2 = 100\ \text{k}\Omega$, $R_{x1} = 1\ \text{k}\Omega$

and $R_{x2} = 100\ \mathrm{k}\Omega$, leading to $R_{eq} = 1\ \mathrm{k}\Omega, C_{eq} = 1\,\mathrm{nF}$. The frequency response of the circuit in Fig. 11 is illustrated in Fig. 12, and the figure shows that the centre frequency f_c, for the band-pass response can be electronically tuned by changing the dc bias current I_{B2}.

4 Conclusion

In this article, a CC-CFA-based grounded lossy capacitance multiplier and an FDNR simulator are presented. The proposed configuration uses two CC-CFAs as an active element, and grounded capacitors or resistors as passive elements. The passive component matching conditions do not require to obtain the considered impedance simulators. The impedance values can be electronically adjusted by changing the dc bias current of the CC-CFAs, and the active and passive sensitivity of the proposed impedance simulator is low. The proposed lossy impedance simulator was tested in an R-L-C second-order notch filter, a fifth-order elliptic low-pass filter, and an R-L-C second-order resonance circuit. Our theoretical analysis of the circuit was verified using a PSPICE simulation model. The proposed electronically tunable configurations (based on a large-value capacitance and FDNR) were shown to be suitable for the design an integrated circuit for signal processing and generation.

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