SERBIAN JOURNAL OF ELECTRICAL ENGINEERING
Vol. 17, No. 3, October 2020, 259-283

UDC: 621.382.3; 621.3.049 **DOI: https://doi.org/10.2298/SJEE2003259G**

Novel Reversible CLA, Optimized RCA and Parallel Adder/Subtractor Circuits

Mohammad Samadi Gharajeh[1], Majid Haghparast[2]

Abstract: This paper proposes reversible circuit designs of the three most commonly used adders: carry look-ahead adder (CLA adder), ripple carry adder (RCA adder), and parallel adder/subtractor. The n-bit reversible CLA adder, called CLA-GH, is designed using the Peres and Fredkin gates. The n-bit optimized reversible RCA adder, called ORCA-GH, is designed using the reversible circuit of a parity-preserving reversible full adder. Both circuits reduce the quantum cost. However, the ORCA-GH circuit also improves the number of constant inputs. Furthermore, the n-bit reversible parallel adder/subtractor, called PAS-GH, is designed using the Feynman, Peres, and Fredkin gates. It decreases the number of garbage outputs and quantum cost. The transistor realizations of the CLA-GH and PAS-GH circuits are provided accordingly. The evaluation results indicate that the proposed circuits surpass the existing works in all figures of merit.

Keywords: Reversible Circuit Design, Carry Look-ahead Adder, Ripple Carry Adder, Parallel Adder/Subtractor.

1 Introduction

Reversible circuit computing [1, 2, 50, 51] has already been applied in lossless classical computing [3, 52] and quantum computing [4, 5, 53]. It can implement both classical and quantum hardware technologies. The reversible circuit design can be differentiated from the arbitrary circuit design with respect to two main characteristics: (i) the number of outputs is equal to the number of inputs and (ii) the corresponding output expressions are not the same for any pair of different input expressions. For example, it is clear that an OR gate is not a reversible gate for two reasons: (i) it includes only one output while having two inputs; (ii) the output expressions (i.e., '1') are not different for the three different input expressions (i.e., '01', '10' and '11') [6]. Therefore, the classical logic design can be transformed into a reversible circuit design to be applied in nanotechnology systems.

[1]Young Researchers and Elite Club, Tabriz Branch, Islamic Azad University, Tabriz, Iran; E-mail: m.samadi@iaut.ac.ir; mhm.samadi@gmail.com
[2]Department of Computer Engineering, Yadegar-e-Imam Khomeini (RAH) Shahre Rey Branch, Islamic Azad University, Tehran, Iran; E-mail: haghparast@srbiau.ac.ir

In recent decades, researchers have discussed the main characteristics of classical logic and reversible logic. They mentioned that any bit of the data lost in irreversible logic circuits generates $kT\ln 2$ joules of heat energy, where k indicates the Boltzmann constant and T indicates absolute temperature [7]. In contrast, the reversible circuit does not lose any data and, therefore, $kT\ln 2$ joules of the heat energy will be reserved in reversible logic circuits [8]. In addition, the voltage-coded logic contains an energy of $E_{sig} = 1/2CV^2$, so that this energy is not reserved whenever the code voltage is adjusted in irreversible CMOS technology. Consequently, it is clear that the reversible circuit design leads to preserving energy in nanotechnology systems [9].

In the last decades, some of the arithmetic operations such as multiplication [10, 11], counter [12, 13], and division [14] are designed as reversible circuits that would be applied in some nanotechnology systems. The optimized and fault-tolerant design of reversible barrel shifters is presented by Shamsujjoha et al. [40], which applies low power MOS transistors. Programmable Logic Array (PLA) is one of the main programmable circuits in the process of implementing combinational circuits. Tara and Babu [41] provided a synthesis for a reversible PLA based on products sharing. Misra et al. [42] discussed the design of efficient reversible binary code converters and a dual-rail checker for emerging nanocircuits. Quantum Cellular Automata (QCA) technology is one of the most popular solutions for transforming current technologies into quantum technology. A reversible Arithmetic Logic Unit (ALU) is designed by Naghibzadeh and Houshmand [43] using QCA cells so that the implementation process is enhanced by the evaluation parameters. In addition, Kianpour and Sabbaghi-Nadooshan [44] suggested an 8-bit reversible full adder/subtractor, which applies QCA reversible circuit technology.

Adder and adder/subtractor [15] are two main components in arithmetic operations (e.g., multiplication and division). Therefore, they can be designed and implemented as reversible circuits on a quantum scale. The existing reversible adder and adder/subtractor circuits, in most cases, are not efficient, so that the number of constant inputs, the number of garbage outputs, and quantum cost are not adequately low. For this reason, in this paper, we propose two circuits of the reversible adder using ripple carry adder (RCA adder) [16, 17] and carry look-ahead adder (CLA adder) [18 − 20], as well as a reversible adder/subtractor using a parity-preserving reversible full adder and RCA adder. It is worth noting that some of the basic reversible gates, including Feynman gate, Peres gate, and Fredkin gate, are used in the internal architectures of the proposed circuits. The main objective of this work is to design the adder and adder/subtractor circuits in such a way that the number of constant inputs and the number of garbage outputs are decreased, and the quantum cost is efficiently reduced.

Computational logic can be considered as sequences of performing arithmetic operations (e.g., addition and subtraction) on computer and digital systems. Efficient arithmetic operation can decrease operational complexity and execution delay. As adder and subtractor are two main components to perform basic arithmetic operations of computer and digital systems, they must be designed and implemented efficiently to reduce delay and complexity [48]. In reversible logic, complexity and delay would be reduced by decreasing the number of constant inputs, the number of garbage outputs, and quantum cost [13]. Consequently, the main objective of this paper is to propose reversible circuits for adder and subtractor to decrease the number of constant inputs, the number of garbage outputs, and quantum cost in comparison with the existing works. It seems that this work could improve the performance of the reversible adder and subtractor circuits in term of computational techniques.

The rest of this paper is organized as follows. Block diagrams, quantum representations, and transistor realizations of the basic reversible and quantum gates are represented in Section 2. The architectures and internal circuits of the proposed reversible adder and adder/subtractor are described in Section 3. The proposed circuits are evaluated in Section 4 in term of the total logical calculation. They are compared to some of the existing works in Section 5 in terms of the number of constant inputs, the number of garbage outputs, and quantum cost. Section 6 includes the process of simulating the proposed circuits using VHDL codes. Finally, the paper is concluded in Section 7.

2 Background

This section considers the main characteristics, block diagrams, quantum representations, and transistor realizations of the basic reversible circuits that are used in the reversible circuits proposed in this paper. In addition, the main characteristics of the quantum circuits are discussed at the end of the section.

A function with n inputs and n outputs can be reversible if, and only if, there is a one-to-one correlation between inputs and outputs. In fact, the input vector can be markedly recovered from the output vector, and vice versa. A n×n reversible gate can be defined as below

$$I_v = (I_1, I_2, \ldots, I_n),$$

$$O_v = (O_1, O_2, \ldots, O_n),$$

where I_v and O_v are the input and output vectors, respectively. NOT gate, Feynman gate [21], Peres gate [22], and Fredkin gate [24, 28] are some of the most popular reversible logic gates. The block diagrams, output equations, quantum representations, and transistor realizations of these gates are described below.

NOT gate is the basic reversible gate, as it is a 1×1 logic gate. Fig. 1 shows a schematic of the NOT gate. The quantum cost of this gate is equal to 1.

Fig. 1 – *Elements of the NOT gate.*

Feynman gate (FG) is a 2×2 reversible gate, also known as a controlled-not gate (CNOT). The output expressions of the gate are defined as

$$P = A;\ Q = A \oplus B, \tag{1}$$

where A is the control bit, B is the target bit, P and Q are the output bits. These expressions indicate that the target output (Q) is the inverse of B when the control bit is equal to 1. Furthermore, it is the same as B when the control bit is 0. The FG gate can also be used to make a copy of any signal. The quantum cost of this gate is 1. Fig. 2 illustrates the block diagram, quantum representation, and transistor realization of this gate.

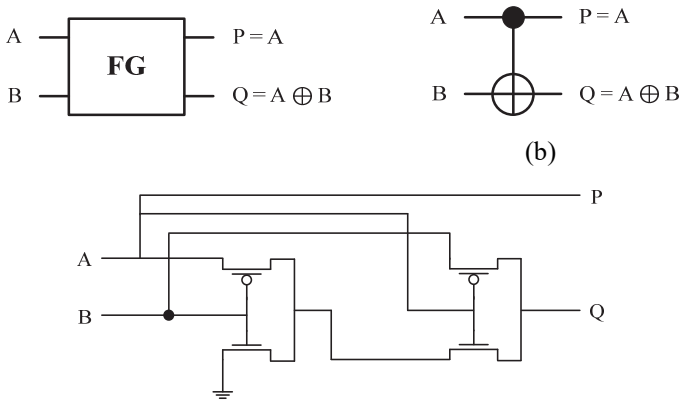


Fig. 2 – *Elements of the Feynman gate [21]: (a) Block diagram; (b) Quantum representation; (c) Transistor realization [41].*

Peres gate (PG) is a 3×3 reversible gate built by a Toffoli gate [23] followed by a FG gate. The output expressions of the gate are represented as below

$$P = A;\ Q = A \oplus B;\ \ R = AB \oplus C, \tag{2}$$

where A, B, and C indicate the inputs, as well as P, Q, and R indicate the outputs. The PG gate is also a universal gate. so it includes a quantum cost of 4. Fig. 3 shows the block diagram, quantum representation, and transistor realization of this gate.

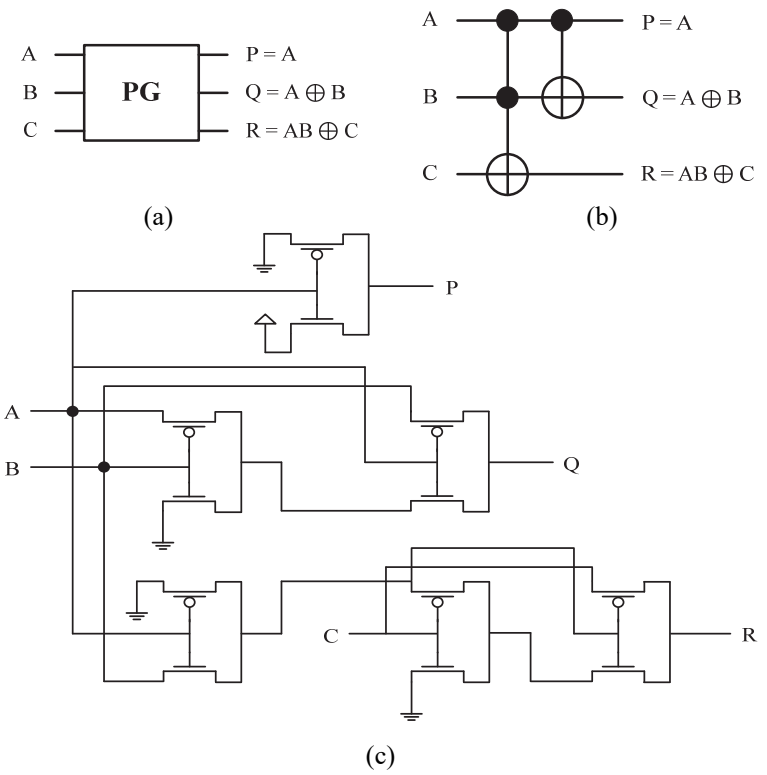


Fig. 3 – *Elements of the Peres gate* [22]: (a) *Block diagram*; (b) *Quantum representation*; (c) *Transistor realization* [47].

Fredkin gate (FRG) is a 3×3 reversible logic gate, which is also known as a controlled permutation gate. The output expressions of this gate are defined as follows

$$P = A;\ Q = A'B \oplus AC;\ R = A'C \oplus AB\,, \tag{3}$$

where A, B, and C are the inputs, as well as P, Q, and R are the outputs. Since the Hamming weight of the input bits is equal to that of the output bits, this gate is a conservative logic gate. Fig. 4 depicts the block diagram, quantum representation, and transistor realization of the FRG gate. It is worth noting that the quantum cost of this gate is equal to 5.

A quantum gate is derived from the theory of quantum computing. It operates on small units of quantum data, called qubits. A qubit can be formulated by a two-dimensional vector. Quantum gates can be illustrated by unitary matrices [25, 26]. The quantum gate of a qubit can be defined by a 2×2 unitary matrix. Hadamard gate is a quantum gate, which operates using an individual qubit. It is represented by the Hadamard matrix as below:

$$H = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \tag{4}$$

where the H matrix is a unitary matrix, as the rows are orthogonal.

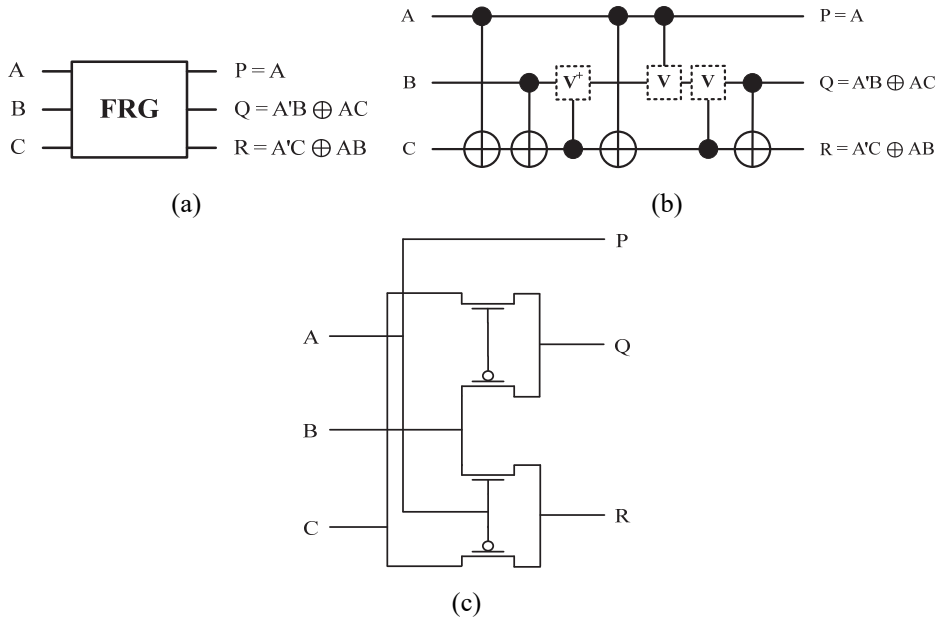


Fig. 4 – *Elements of the Fredkin gate* [24, 28]: (a) *Block diagram;* (b) *Quantum representation;* (c) *Transistor realization* [40].

In controlled-V, if the control signal (A) is equal to 0, the second output (Q) will be equal to B. In addition, if the input A is equal to 1, the output Q will be equal to V(B). The arithmetic representation of V can be represented as

$$V = \left[\frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}\right]. \tag{5}$$

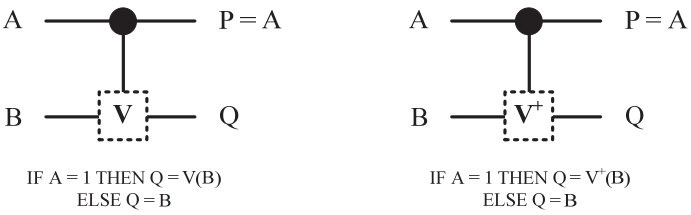
In controlled-V^+, if the control input (A) is equal to 0, the second output (Q) will be equal to B. Moreover, if the input A is equal to 1, the output Q will be equal to V^+(B).

Fig. 5 shows the quantum representations of the controlled-V and controlled-V^+ gates. V and V^+ are some of the most popular quantum gates. The arithmetic expressions of this gate [27] can be represented as below

$$V \times V = NOT\,, \tag{6}$$

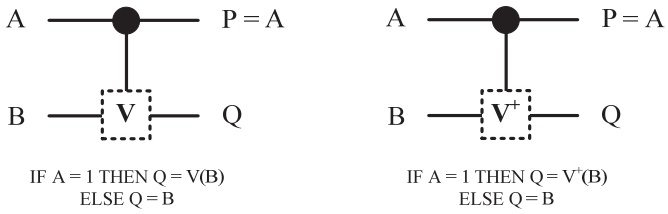
$$V \times V^+ = V^+ \times V = I\,, \tag{7}$$

$$V^+ \times V^+ = NOT\,. \tag{8}$$



(a) (b)

Fig. 5 – *Elements of the controlled-V and controlled-V+ gates:*
(a) *Quantum representation of the controlled-V gate;*
(b) *Quantum representation of the controlled-V+ gate.*



(a) (b)

Fig. 5 – *Elements of the controlled-V and controlled-V+ gates:*
(a) *Quantum representation of the controlled-V gate;*
(b) *Quantum representation of the controlled-V+ gate.*

3 The Proposed Reversible Circuits

This section describes the reversible circuits of the proposed n-bit CLA adder, the optimized n-bit RCA adder, and the n-bit adder/subtractor. These circuits are explained in the following subsections.

3.1 CLA-GH: the proposed reversible CLA adder

One of the most important mechanisms to improve the performance of initial adders was to reduce the delay in the carry propagation. The CLA adder calculates the carry signals in advance based on the input signals to solve the above problem. Fig. 6 shows a general representation and the internal circuit of the CLA adder to calculate the addition of the operand bits in stage i, denoted by A_i and B_i, and the carry bit from the previous stage, where $i = \{0, 1, \ldots, n\text{-}1\}$. Adder operations are performed based on the fact that a carry signal can be generated in two cases: (i) when the bits of A_i and B_i are equal to 1, or (ii) when one of these bits is equal to 1, as well as the carry bit from the previous stage is equal to 1. P_i is known as a carry propagate signal in which the input carry is propagated to the output carry whenever P_i equals 1. G_i is known as a carry generate signal in which the output carry (C_{i+1}) is generated whenever G_i is 1 without considering the input carry (C_i).

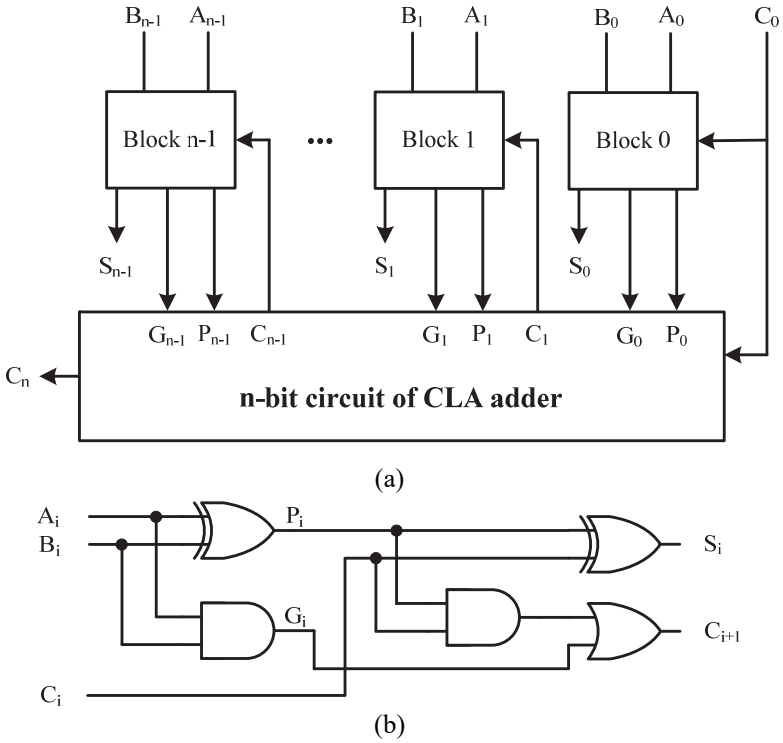


Fig. 6 – *A schematic of the CLA adder:* (a) *An overall viewpoint of the adder built by n-bit blocks;* (b) *Inner circuit of block i.*

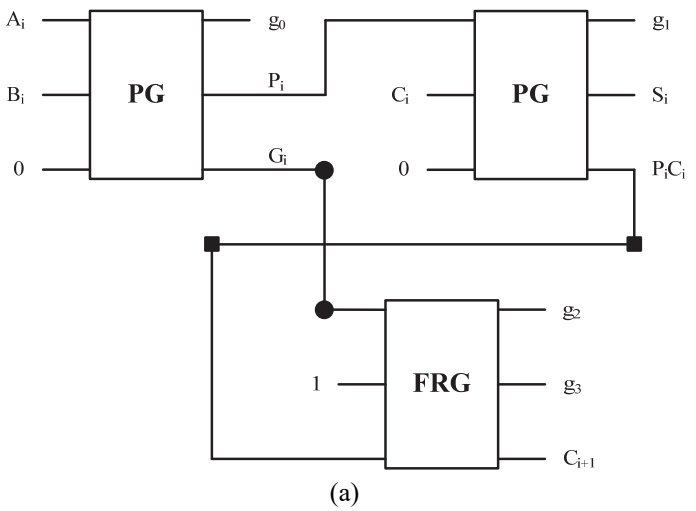


Fig. 7 – *The proposed reversible circuit for any block in the CLA-GH circuit*: (a) *Reversible architecture of block i.*

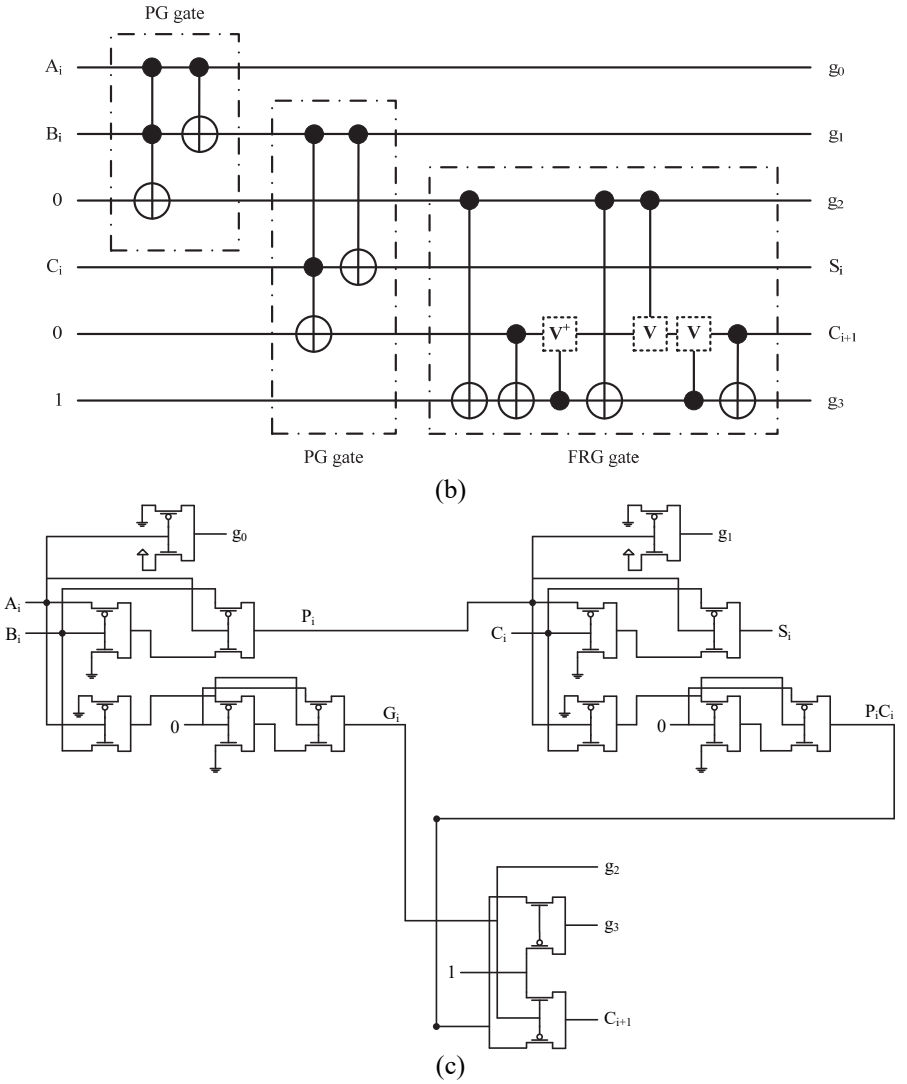


Fig. 7 – *The proposed reversible circuit for any block in the CLA-GH circuit:* (b) *The implemented circuit of block i;* (c) *Transistor realization of block i.*

Therefore, P_i and G_i can be formulated as follows:

$$P_i = A_i \oplus B_i , \tag{9}$$

$$G_i = A_i B_i . \tag{10}$$

In addition, the output sum and carry bits can be given by:

$$S_i = P_i \oplus C_i , \tag{11}$$

$$C_{i+1} = G_i + P_i C_i . \tag{12}$$

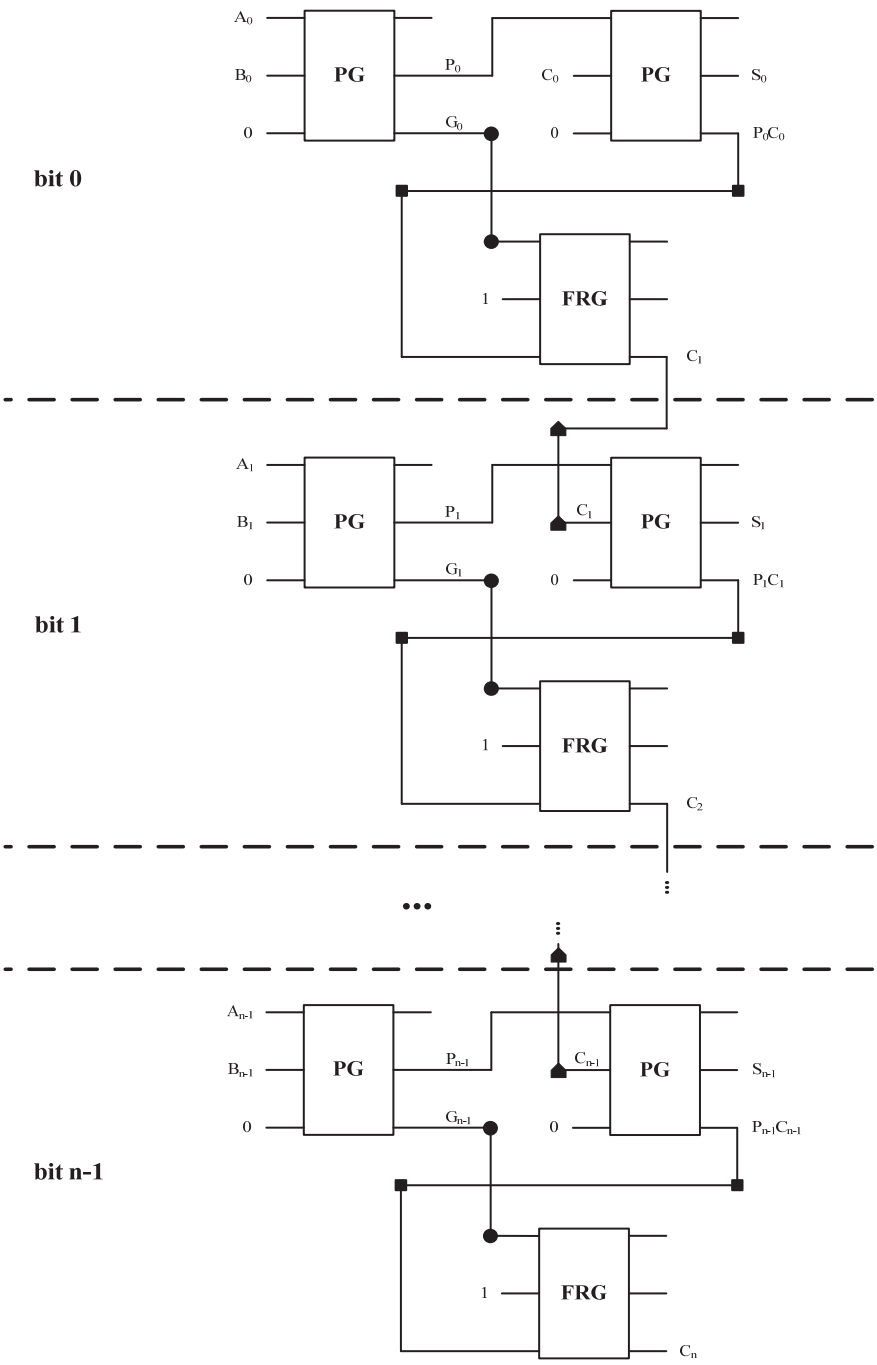


Fig. 8 – *Architecture of the proposed reversible circuit for n-bit CLA-GH circuit.*

We propose a reversible CLA adder, called CLA-GH, which uses the PG and FRG gates in the implemented circuit. As shown in Fig. 7a, each reversible block of the adder consists of two PG gates and one FRG gate. The first PG gate generates P_i and G_i, the second PG gate generates S_i and P_iC_i, as well as the FRG gate generates C_{i+1} where $i = \{0,1,\ldots,n\text{-}1\}$. Fig. 7b illustrates the implemented circuit and the synthesis process of block *i*. It indicates that the proposed circuit has six inputs, six outputs, three constant inputs, and four garbage outputs. Furthermore, Fig. 7c represents the transistor realization of block *i* based on the transistor realizations of the PG and FRG gates.

The reversible circuit of the proposed *n*-bit CLA-GH circuit is shown in Fig. 8. The proposed architecture for each block is repeated for the entire gate in n stages. The output carry of each stage is connected to the input carry bit of the next stage. Consequently, the number of constant inputs, the number of garbage outputs, and the quantum cost of the proposed *n*-bit CLA-GH circuit are calculated as

$$C_{\text{CLA-GH}} = 3n, \quad G_{\text{CLA-GH}} = 4n, \quad QC_{\text{CLA-GH}} = 13n, \tag{13}$$

where $C_{\text{CLA-GH}}$ is the number of constant inputs, $G_{\text{CLA-GH}}$ is the number of garbage outputs, and $QC_{\text{CLA-GH}}$ is the quantum cost of the proposed circuit.

As the proposed reversible circuit for each block consists of two PG gates and one FRG gate, the quantum cost of the entire circuit can be calculated as $QC_{\text{CLA-GH}} = (2\times QC_{\text{PG}} + 1\times QC_{\text{FRG}})\times n$. Therefore, it can result as $QC_{\text{CLA-GH}} = (2\times 4 + 1\times 5)\times n = 13n$.

3.2 ORCA-GH: the proposed reversible optimized RCA adder

This subsection presents a new reversible optimized RCA adder, called ORCA-GH, to calculate the operation of adding the two n-bit operands. Fig. 9 shows the block diagram and the quantum representation of the parity-preserving reversible full adder [28], called PPFA in this paper. The PPFA gate has two constant inputs and three garbage outputs to determine the addition of the operand bits, denoted by X and Y, and the input carry bit (C_{in}). It calculates the result of the addition, denoted by S, and the output carry bit (C_{out}). As the quantum cost of this gate is equal to 9, it is more efficient than the existing full adder circuits.

Fig. 10 illustrates the general architecture of the proposed *n*-bit ORCA-GH circuit. It uses the PPFA gate to add the operands in stage i, denoted by A_i and B_i, and the carry bit that comes from the previous stage, where $i = \{0,1,\ldots,n\text{-}1\}$. The input carry bit at each stage is connected to the output carry bit of the previous stage. Consequently, the number of constant inputs, the number of garbage outputs, and the quantum cost of the proposed n-bit ORCA-GH circuit are specified as follows

$$C_{\text{ORCA-GH}} = 2n, \quad G_{\text{ORCA-GH}} = 3n, \quad QC_{\text{ORCA-GH}} = 9n, \tag{14}$$

where $C_{ORCA\text{-}GH}$ is the number of constant inputs, $G_{ORCA\text{-}GH}$ is the number of garbage outputs, and $QC_{ORCA\text{-}GH}$ is the quantum cost of the proposed circuit.

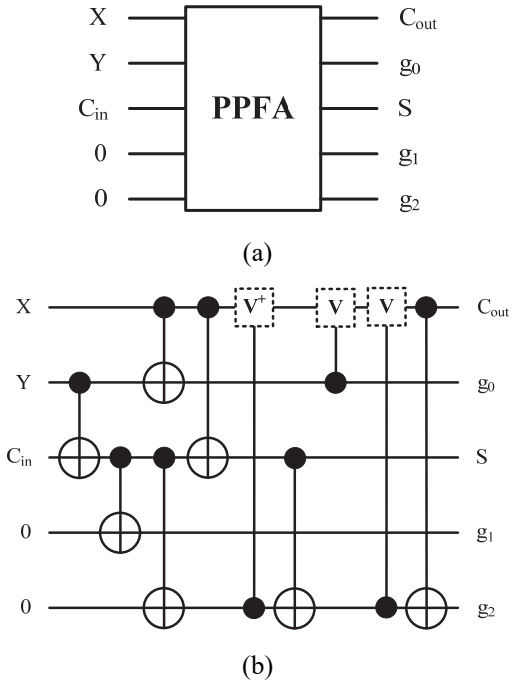


Fig. 9 – *Elements of the PPFA gate* [28]:
(a) *Block diagram*; (b) *Quantum representation*.

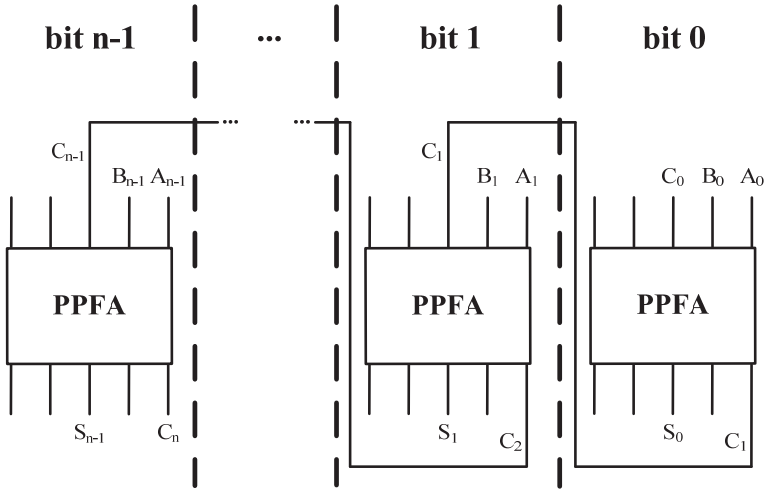


Fig. 10 – *Inner structure of the proposed reversible circuit for the n-bit ORCA-GH circuit.*

3.3 PAS-GH: the proposed reversible parallel adder/subtractor

An adder/subtractor circuit contains both the adder circuit and the subtractor circuit, cooperatively. It can be represented based on the following calculations

$$S = A + B,\ C_{in} = 0\ , \tag{15}$$

$$D' = A - B = A + \overline{B} + 1 \overset{yields}{\rightarrow} D = A + \overline{B},\ C_{in} = 1\ , \tag{16}$$

where A and B are the operands, C_{in} is the input carry of the first bit, S is the sum of the operands, and D is the difference of the operands. The proposed reversible parallel adder/subtractor, called PAS-GH, is considered as an extended circuit of the CLA adder.

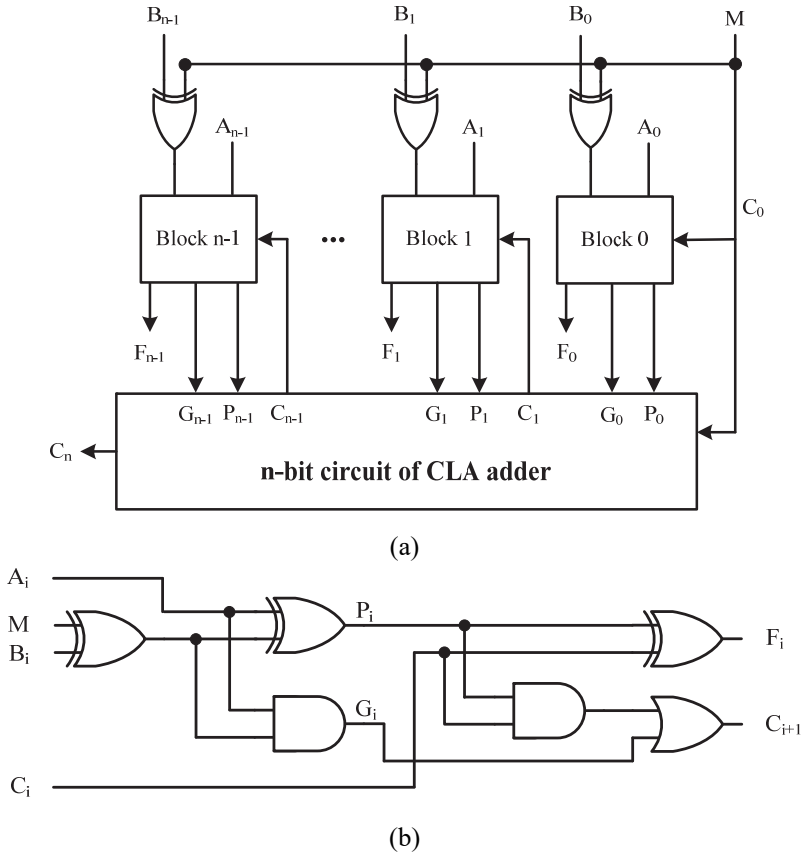


Fig. 11 – *An overall view of the n-bit parallel adder/subtractor*:
(a) *The extended block diagram of the CLA adder for the adder/subtractor circuit*;
(b) *Internal structure of block i*.

Fig. 11a shows an extended block diagram of the CLA adder for the n-bit adder/subtractor circuit. A mode bit, denoted by M, is incorporated into the previous circuit to determine whether the addition or subtraction operation will be operated by the circuit or not. If M=0, the addition operation will be operated. Otherwise, the subtraction operation will be performed. Note that it is connected to the input carry of the first stage (C_0). Fig.11b represents the internal architecture of block *i* in the adder/subtractor circuit. It is designed to add or subtract the operands in stage *i*, denoted by A_i and B_i, and the carry bit generated by the previous stage where $i = \{0, 1, \ldots, n\text{-}1\}$. Therefore, P_i and G_i can be defined as follows:

$$P_i = A_i \oplus (M \oplus B_i), \tag{17}$$

$$G_i = A_i (M \oplus B_i). \tag{18}$$

In addition, the result of addition or subtraction, as well as the output carry can be determined as

$$F_i = P_i \oplus C_i, \tag{19}$$

$$C_{i+1} = G_i + P_i C_i. \tag{20}$$

The PAS-GH circuit consists of the FG, PG, and FRG gates. Fig. 12a shows that every reversible block of the adder is designed by one FG gate, two PG gates, and one FRG gate. The FG gate performs the XOR operation between M and the second operand, the first PG gate generates P_i and G_i, the second PG gate generates F_i and P_iC_i, as well as the FRG gate generates C_{i+1} where $i = \{0, 1,\ldots, n\text{-}1\}$. Fig. 12b shows the quantum representation of each block in the proposed circuit. It illustrates that the implemented adder/subtractor circuit consists of seven inputs, seven outputs, three constant inputs, and five garbage outputs.

Moreover, Fig. 12c illustrates the transistor realization of block *i* based on the transistor realizations of the FG, PG, and FRG gates.

Fig. 13 shows the reversible architecture of the *n*-bit PAS-GH circuit.

The proposed structure for each block is replicated in n stages. In contrast to the reversible circuit of block i represented by Fig. 12, the garbage outputs of all FG gates in the n-bit circuit, except bit n-1, are eliminated from the circuit by connecting the garbage output of each FG gate for the first input bit (M) of the FG gate in the next stage. In addition, an extra FG gate with a constant input is applied at bit 0 to propagate M to the first input carry (C_0) and FG gate of bit 0. Therefore, the number of constant inputs, the number of garbage outputs, and the quantum cost of the n-bit PAS-GH circuit are calculated as follows:

$$C_{\text{PAS-GH}} = 3n+1, \quad G_{\text{PAS-GH}} = 4n+1, \quad QC_{\text{PAS-GH}} = 14n+1, \tag{21}$$

where $C_{\text{PAS-GH}}$ is the number of constant inputs, $G_{\text{PAS-GH}}$ is the number of garbage outputs, and $QC_{\text{PAS-GH}}$ is the quantum cost of the proposed circuit.

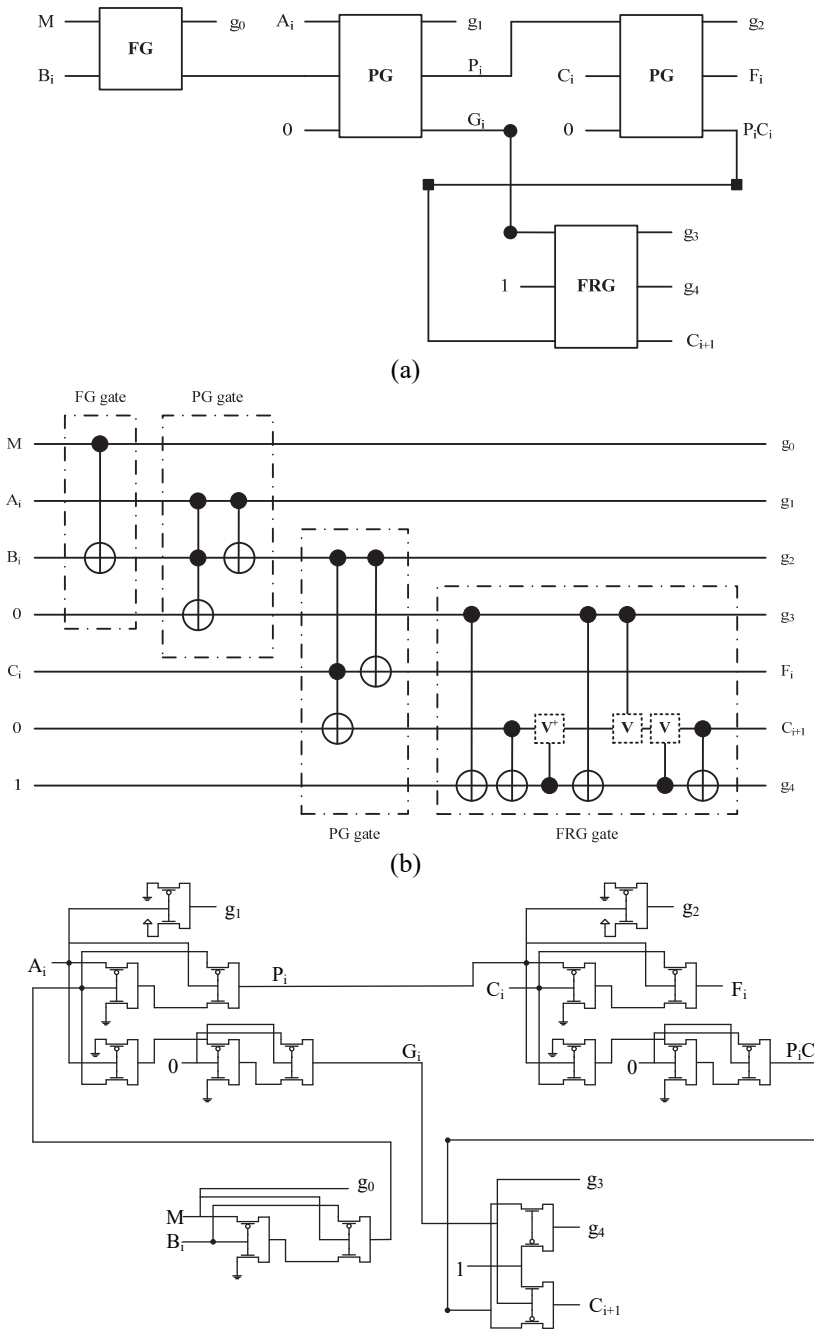


Fig. 12 – *The proposed reversible circuit for each block of the PAS-GH circuit:* (a) *Reversible block diagram of each block;* (b) *Quantum representation of block i;* (c) *Transistor realization of block i.*

As each block of the n-bit PAS-GH circuit consists of one FG gate, two PG gates, and one FRG gate, the quantum cost of each block can be calculated as

$$QC = \left(1 \times QC_{FG} + 2 \times QC_{PG} + 1 \times QC_{FRG}\right) = \left(1 \times 1 + 2 \times 4 + 1 \times 5\right) = 14 .$$

As an extra FG gate is applied to the first bit, the quantum cost of the n-bit PAS-GH circuit is defined as $QC_{PAS\text{-}GH} = 14n + 1$.

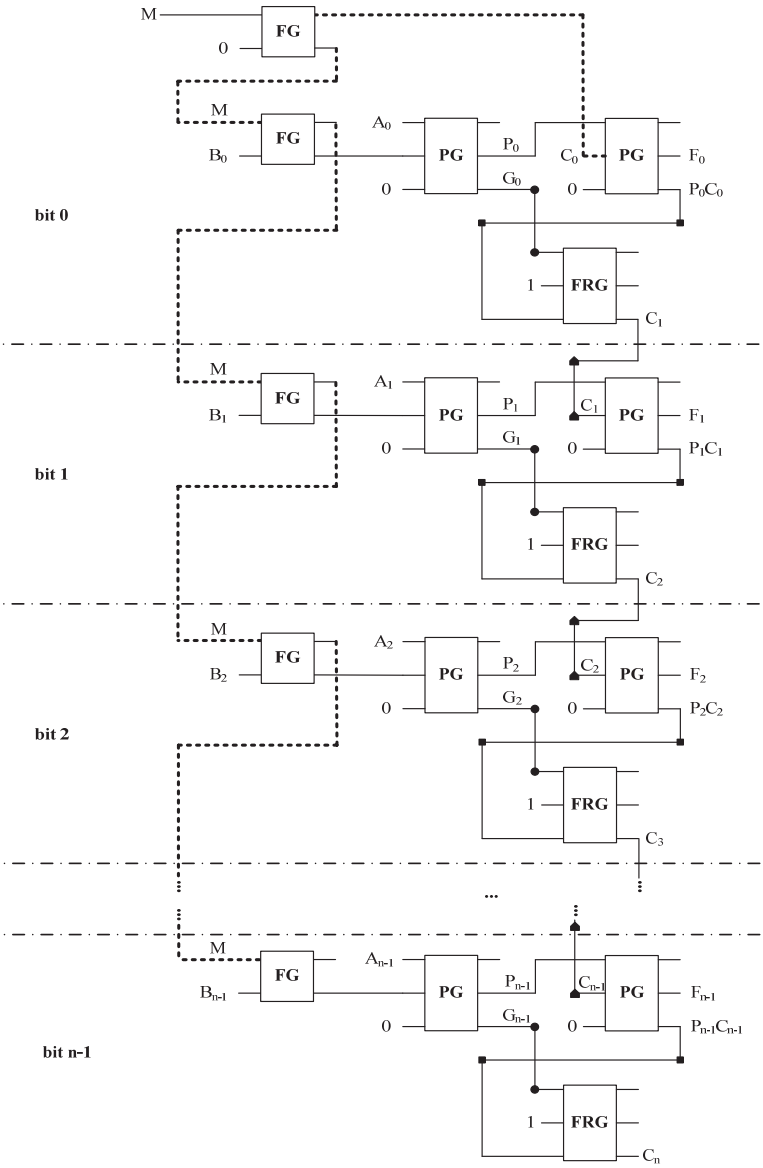


Fig. 13 – *Architecture of the proposed n-bit PAS-GH circuit.*

4 Performance Evaluation

The performance evaluations of the proposed adder and adder/subtractor circuits are represented in **Tables 1**, **2** and **3**. Hardware complexity is one of the important features in circuit design. Total logical calculation is a technique for calculating the hardware complexity of any designed circuit. It indicates the number of the XOR, AND, NOT operations in the output expressions. Suppose α indicates an EX-OR gate calculation with two inputs, β indicates an AND gate calculation with two inputs, γ indicates a NOT gate calculation, and T indicates total logical calculation.

Since the proposed reversible circuits apply some of the basic reversible gates, the total logical calculations for these gates are determined initially and then the total logical calculations of the proposed circuits are calculated separately. The FG gate has an XOR in the output expressions. Therefore, the total logical calculation of this gate is indicated as $T_{FG} = 1\alpha$. The PG gate contains two XORs and an AND in the output expressions. Thus, the total logical calculation of this gate is represented as $T_{PG} = 2\alpha + 1\beta$. The FRG gate involves two XORs, four ANDs, and two NOTs in the output expressions. Therefore, the total logical calculation of this gate is specified as

$$T_{FRG} = 2\alpha + 4\beta + 2\gamma .$$

Each block of the proposed CLA-GH circuit consists of two PG gates and one FRG gate. The total logical calculation of each block in this circuit is calculated as:

$$T = 2 \times T_{PG} + 1 \times T_{FRG} = 2 \times (2\alpha + 1\beta) + 1 \times (2\alpha + 4\beta + 2\gamma) = 6\alpha + 6\beta + 2\gamma.$$

Consequently, the total logical calculation of the n-bit CLA-GH circuit is determined as $T_{CLA\text{-}GH} = n(6\alpha + 6\beta + 2\gamma)$. **Table 1** represents the specifications of the CLA-GH circuit.

Table 1
Specification of the proposed CLA-GH circuit.

Basic gate	The number of constant inputs	The number of garbage outputs	Quantum cost	Total logical calculation
PG, FRG	3n	4n	13n	n(6α + 6β + 2γ)

As shown in [28], the PPFA gate has thirteen XORs, four ANDs, and two NOTs in the output expressions. Therefore, the total logical calculation of the PPFA gate can be obtained as $T_{PPFA} = 13\alpha + 4\beta + 2\gamma$. Accordingly, the total logical calculation of the n-bit ORCA-GH circuit is specified as **Table 2** expresses the specifications of the ORCA-GH circuit.

Table 2
Specification of the proposed ORCA-GH circuit.

Basic gate	The number of constant inputs	The number of garbage outputs	Quantum cost	Total logical calculation
Not Reported	2n	3n	9n	n(13α + 4β + 2γ)

Each block of the proposed PAS-GH circuit consists of one FG gate, two PG gates, and one FRG gate. In addition, an extra FG gate is applied to the first bit of the circuit. The total logical calculation of each block in this circuit is determined as:

$$T = 1\times T_{FG} + 2\times T_{PG} + 1\times T_{FRG} =$$
$$= 1\times(1\alpha) + 2\times(2\alpha + 1\beta) + 1\times(2\alpha + 4\beta + 2\gamma) =$$
$$= 7\alpha + 6\beta + 2\gamma.$$

As a result, the total logical calculation of the n-bit PAS-GH circuit is completed as $T_{PAS\text{-}GH} = n(7\alpha + 6\beta + 2\gamma) + \alpha$. **Table 3** represents the specifications of the PAS-GH circuit.

Table 3
Specification of the proposed PAS-GH circuit.

Basic gate	The number of constant inputs	The number of garbage outputs	Quantum cost	Total logical calculation
FG, PG, FRG	3n+1	4n+1	14n+1	n (7α + 6β + 2γ) + α

5 Comparison Results

The proposed reversible adders are compared with some of the existing adders based on the quantum cost of the implemented circuits.

Table 4 represents the quantum costs of the reversible adder circuits. These results are carried out based on the evaluation results of the 4-bit, 8-bit, 16-bit, and 32-bit adder circuits. They indicate that the quantum costs obtained by the proposed CLA-GH and ORCA-GH circuits are efficient, in most cases, compared to the existing reversible adders. Moreover, the number of constant inputs achieved by the ORCA-GH circuit can be improved by almost 10% compared to Ref. [32]. As the quantum costs of some existing adders have not been clearly defined by the authors, their quantum costs are obtained according to the results of Ref. [36].

Ref. [49] presents two designs of the adder circuit. The evaluation results indicate that the efficiency of the proposed ORCA-GH circuit is the same as that of Ref. [49] – Design I. In contrast, the performance of the ORCA-GH circuit is better than that of Ref. [49] – Design II based on the quantum cost.

Note that the adder circuits shown in Ref. [49] are suggested only for the 4-bit adder, while the proposed adder circuit is applicable to the n-bit adder.

Table 4

Comparison results between quantum costs of the reversible adder circuits.

Adder	n-bit	4-bit	8-bit	16-bit	32-bit
Design 2 ORCA-GH circuit	9n	36	72	144	288
Design 1 (CLA-GH circuit)	13n	52	104	208	416
Ref. [49] – Design I	Not Reported	36	Not Reported	Not Reported	Not Reported
Ref. [49] – Design II	Not Reported	43	Not Reported	Not Reported	Not Reported
Ref. [29]	$>\lceil (9/4)n^2+(15/4)n-1\rceil$	50	173	635	2423
Ref. [30]	15n-9	51	111	231	471
Ref. [31]	16n-10	54	118	246	502
Ref. [32]	6(2n+1)	54	102	198	390
Ref. [33]	17n-12	56	124	260	532
Ref. [34]	$3n^2+2n$	56	208	800	3136
Ref. [35]	26n-29	75	179	387	803
Ref. [36]	$49\lceil n/4\rceil+92\lceil n/16\rceil+13$	85	157	301	589
Ref. [37]	$\lceil n/4\rceil\times 165$	165	330	660	1320
Ref. [38]	57n-3	225	453	909	1821
Improvement of Design 1		(0-77)%	(0-77)%	(0-77)%	(0-87)%
Improvement of Design 2		(0-84)%	(29-84)%	(27-84)%	(26-91)%

Table 5 represents the analysis results of the 8-bit reversible adder/ subtractor circuits. These results indicate that the number of garbage outputs obtained by the PAS-GH circuit proposed for 8-bit adder/subtractor circuit can be decreased by almost 13% compared to that obtained by [39] – Design I. Furthermore, the quantum cost of the proposed circuit can be reduced by almost (29 – 67)% compared to the other adder/subtractor circuits.

Ref. [45] presents a quantum ternary parallel adder/subtractor in which each digital bit is implemented by a ternary full-adder. Each ternary full-adder in this design uses three FG gates and six Toffoli gates. Since the quantum cost of the FG gate is 1 and the quantum cost of the Toffoli gate is 5, the quantum cost of the n-bit quantum parallel adder/subtractor in Ref. [45] is equal to $(3\times1 + 6\times5)\times n = 33n$.

Ref. [46] suggests a quantum ternary full adder to perform a n-bit quantum adder circuit, as well as a ternary full subtractor to perform a n-bit quantum subtractor circuit. These circuits are designed to run a n-bit quantum adder/subtractor separately. The authors indicated that the cost of the suggested ternary full adder is 50 and the cost of the suggested ternary full subtractor is 35. Therefore, we consider an average value of these costs to be 43n to drive the comparison results.

The proposed reversible circuit is, in fact, a binary adder/subtractor circuit. Therefore, we compare it with the only existing adder/subtractor circuit presented in Ref. [39] – Design I. As we tried to analyze the efficiency of the proposed adder/subtractor circuit compared to the quantum adder/subtractor circuits, the proposed circuit was compared to the quantum adder/subtractor circuits presented in Ref. [45] and Ref. [46].

Table 5

Comparison results of the 8-bit reversible adder/subtractor circuits.

Adder/subtractor circuits	Type	The number of garbage outputs	Quantum cost
PAS-GH circuit	Binary	33	113
Ref. [39] – Design I	Binary	38	159
Ref. [45]	Ternary	Not Reported	264
Ref. [46]	Ternary	Not Reported	344
Improvement	-	13%	(29-67)%

6 Simulation Results

This section assesses the simulation results of the proposed reversible circuits using VHDL codes. All circuits are simulated by VHDL codes in Active-HDL v8.3 SP1. Since four simulation results can be performed in the simulation process (three results for addition and one result for subtraction), this section evaluates only three results that are obtained with the addition operation. These results are achieved by the addition operation between two 4-bit numbers for the CLA adder, the RCA adder, and the adder/subtractor circuits. As seen in Fig. 14, the same input data are entered into the waveform to demonstrate that all circuits are working correctly.

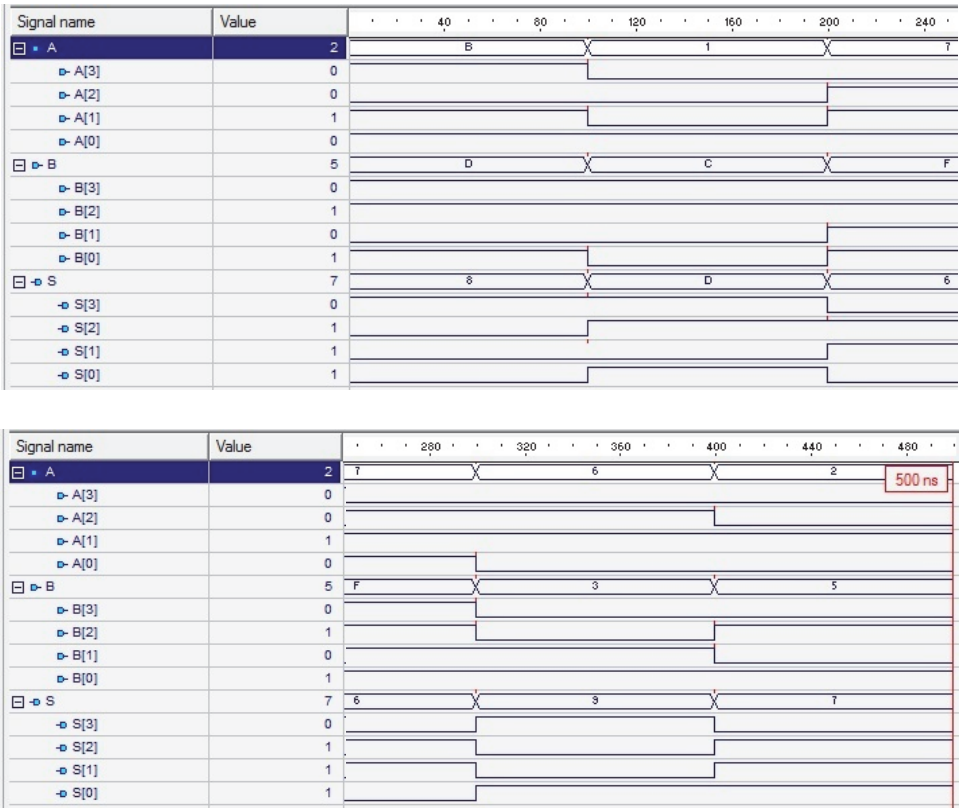


Fig. 14 – *Simulation results of the proposed reversible circuits to add two 4-bit numbers.*

The simulation results are performed for four inputs to calculate the outputs, as represented below

$$S(1000) = A(1011) + B(1101),$$
$$S(1101) = A(0001) + B(1100),$$
$$S(0110) = A(0111) + B(1111),$$
$$S(1001) = A(0110) + B(0011),$$
$$S(0111) = A(0010) + B(0101).$$

7 Conclusion

In this paper, we proposed two reversible adder circuits and a reversible adder/subtractor circuit. An n-bit reversible adder circuit, called CLA-GH, applies the carry look-ahead adder to operate the addition of two n-bit operands. It uses the Peres and Fredkin gates in the implemented circuit. Another n-bit reversible adder circuit, called ORCA-GH, is an optimized ripple carry adder. It uses the circuit of a reversible parity-preserving full adder to perform the addition of two n-bit operand bits. Finally, the n-bit reversible parallel adder/subtractor, called PAS-GH, uses the Feynman, Peres, and Fredkin gates to add or subtract the two n-bit operands.

The performance of the proposed reversible circuits was compared to the most existing works in terms of the number of constant inputs, the number of garbage outputs, and quantum cost. The evaluation results demonstrated that the quantum costs obtained by proposed reversible adders are lower than the costs obtained by the existing reversible adders. Note that the performance of the ORCA-GH circuit is better than the CLA-GH circuit. In addition, the evaluation results indicated that the number of garbage outputs reached by the PAS-GH circuit can be decreased by almost 13% less than that achieved by another reversible adder/subtractor. Furthermore, the quantum cost obtained by this circuit can be reduced by almost (29-67)% less than that obtained by the other adder/subtractor circuits. The reversible circuits proposed for adder and adder/subtractor were considered for n-bit digital systems. In contrast, some of the existing works are applicable only to limited architectures (e.g., 4-bit, 8-bit, or 16-bit).

All the proposed circuits were evaluated by VHDL codes in Active-HDL v8.3 SP1. The evaluation results indicated that the new circuits work correctly for several inputs.

8 References

[1] L. B. Levitin, T. Toffoli: Thermodynamic Cost of Reversible Computing, Physical Review Letters, Vol. 99, No. 11, September 2007, pp. 1 – 5.

[2] A. De Vos: Reversible Computing: Fundamentals, Quantum Computing, and Applications, John Wiley & Sons, Singapore, 2011.

[3] B. Hayes: Computing Science: Reverse Engineering, American Scientist, Vol. 94, No. 2, March/April 2006, pp. 107 – 111.

[4] N. C. Jones, R. Van Meter, A. G. Fowler, P. L. McMahon, J. Kim, T. D. Ladd, Y. Yamamoto: Layered Architecture for Quantum Computing, Physical Review X, Vol. 2, No. 3, September 2012, pp. 031007 – 1 – 031007 – 27.

[5] M. Hirvensalo: Quantum Computing, Springer, 2004.

[6] A. De Vos: Reversible Computer Hardware, Electronic Notes in Theoretical Computer Science, Vol. 253, No. 6, March 2010, pp. 17 – 22.

[7] C. H. Bennett: Logical Reversibility of Computation, IBM Journal of Research and Development, Vol. 17, No. 6, November 1973, pp. 525 – 532.

[8] C. McIvor, M. McLoone, J. V. McCanny: Modified Montgomery Modular Multiplication and RSA Exponentiation Techniques, IEEE Proceedings – Computers and Digital Techniques, Vol. 151, No. 6, November 2004, pp. 402 – 408.

[9] M. P. Frank: Introduction to Reversible Computing: Motivation, Progress, and Challenges, Proceedings of the 2nd Conference on Computing Frontiers (CF '05), Ischia, Italy, May 2005, pp. 385 – 390.

[10] M. Haghparast, S. J. Jassbi, K. Navi, O. Hashemipour: Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology, World Applied Sciences Journal, Vol. 3, No. 6, January 2008, pp. 974 – 978.

[11] S. Kotiyal, H. Thapliyal, N. Ranganathan: Reversible Logic Based Multiplication Computing Unit Using Binary Tree Data Structure, The Journal of Supercomputing, Vol. 71, No. 7, March 2015, pp. 2668 – 2693.

[12] M. Haghparast, M. S. Gharajeh: Design of a Nanometric Reversible 4-Bit Binary Counter with Parallel Load, Australian Journal of Basic and Applied Sciences, Vol. 5, No. 7, July 2011, pp. 63 – 71.

[13] M. S. Gharajeh, M. Haghparast: On Design of a Fault Tolerant Reversible 4-Bit Binary Counter with Parallel Load, Australian Journal of Basic and Applied Sciences, Vol. 6, No. 7, July 2012, pp. 430 – 446.

[14] N. M. Nayeem, A. Hossain, M. Haque, L. Jamal, H. M. H. Babu: Novel Reversible Division Hardware, Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems, Cancun, Mexico, August 2009, pp. 1134 – 1138.

[15] M. Morris Mano, C. R. Kime: Logic and Computer Design Fundamentals, 4th Edition, Prentice Hall, London, 2008.

[16] M. S. K. Lau, K. V. Ling, Y. C. Chu, A. Bhanu: Modeling of Probabilistic Ripple-Carry Adders, Proceedings of the 5th IEEE International Symposium on Electronic Design, Test & Application, Ho Chi Minh City, Vietnam, January 2010, pp. 201 – 206.

[17] V. Pudi, K. Sridharan: Low Complexity Design of Ripple Carry and Brent–Kung Adders in QCA, IEEE Transactions on Nanotechnology, Vol. 11, No. 1, January 2012, pp. 105 – 119.

[18] E. S. Sogomonyan, V. Ocheretnij, M. Gossel: A New Code-Disjoint Sum-Bit Duplicated Carry Look-Ahead Adder for Parity Codes, Proceedings of the 10th Asian Test Symposium, Kyoto, Japan, November 2001, pp. 365 – 370.

[19] G. A. Ruiz, M. Granda: An Area-Efficient Static CMOS Carry-Select Adder based on a Compact Carry Look-Ahead Unit, Microelectronics Journal, Vol. 35, No. 12, December 2004, pp. 939 – 944.

[20] J. Samanta, M. Halder, B. P. De: Performance Analysis of High Speed Low Power Carry Look-Ahead Adder Using Different Logic Styles, International Journal of Soft Computing and Engineering, Vol. 2, No. 6, January 2013, pp. 330 – 336.

[21] R. P. Feynman: Quantum Mechanical Computers, Foundations of Physics, Vol. 16, No. 6, June 1986, pp. 507 – 531.

[22] A. Peres: Reversible Logic and Quantum Computers, Physical Review A, Vol. 32, No. 6, December 1985, pp. 3266v3276.

[23] T. Toffoli: Reversible Computing, Proceedings of the 7th International Colloquium on Automata, Languages, and Programming, Noordwijkerhout, The Netherlands, July 1980, pp. 632 – 644.

[24] E. Fredkin, T. Toffoli: Conservative Logic, International Journal of Theoretical Physics, Vol. 21, No. 3/4, April 1982, pp. 219 – 253.

[25] P. Kaye, R. Laflamme, M. Mosca: An Introduction to Quantum Computing, 1st Edition, Oxford University Press Inc., New York, 2007.

[26] A. Barenco, C. H. Bennett, R. Cleve, D. P. DiVincenzo, N. Margolus, P. Shor, T. Sleator, J. Smolin, H. Weinfurter: Elementary Gates for Quantum Computation, Physical Review A, Vol. 52, No. 5, November 1995, pp. 3457v3467.

[27] H. Thapliyal, N. Ranganathan: Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs, ACM Journal on Emerging Technologies in Computing Systems (JETC), Vol. 6, No. 14, December 2010, pp. 14:1 – 14:31.

[28] M. Haghparast, S. Shoaei: Design of a New Parity Preserving Reversible Full Adder, Journal of Circuits, Systems and Computers, Vol. 24, No. 1, January 2015, pp. 1550006-1 – 1550006-11.

[29] R. Zhou, Y. Shi, M. Zhang, H. Wang: A Novel Reversible ZS Gate and its Application for Optimization of Quantum Adder Circuits, Journal of Circuits, Systems, and Computers, Vol. 20, No. 6, October 2011, pp. 1107 – 1129.

[30] Y. Takahashi, S. Tani, N. Kunihiro: Quantum Addition Circuits and Unbounded Fan-Out, Quantum Information and Computation, Vol. 10, No. 9, September 2010, pp. 872 – 890.

[31] M. B. Ali, T. Hirayama, K. Yamanaka, Y. Nishitani: Design of n-bit Reversible Adder with LNN Architecture, Proceedings of the 12th International Conference on Foundations of Computer Science (FCS), Athens, Greece, May 2016, pp. 32 – 37.

[32] M. Haghparast, A. Patiar: Novel Nanometric Reversible Saturating Adder, International Journal of Physical Sciences, Vol. 6, No. 9, May 2011, pp. 2321 – 2326.

[33] S. A. Cuccaro, T. G. Draper, S. A. Kutin, D. Petrie Moulton: A New Quantum Ripple-Carry Addition Circuit, October 2004, pp. 1 – 9, Available at: https://arxiv.org/abs/quant-ph/0410184v1

[34] L. Jamal, M. Shamsujjoha, H. M. H. Babu: Design of Optimal Reversible Carry Look-Ahead Adder with Optimal Garbage and Quantum Cost, International Journal of Engineering and Technology, Vol. 2, No. 1, January 2012, pp. 44 – 50.

[35] Y. Takahashi, N. Kunihiro: A Linear-Size Quantum Circuit for Addition with no Ancillary Qubits, Quantum Information & Computation, Vol. 5, No. 6, September 2005, pp. 440 – 448.

[36] M.- C. Li, R.- G. Zhou: A Novel Reversible Carry-Selected Adder with Low Latency, International Journal of Electronics, Vol. 103, No. 7, September 2015, pp. 1202 – 1215.

[37] H. Thapliyal, M. B. Srinivas: A Novel Reversible TSG Gate and its Application for Designing Reversible Carry Look-Ahead and Other Adder Architectures, Proceedings of the 10th Asia-Pacific Conference on Advances in Computer Systems Architecture, Singapore, Singapore, October 2005, pp. 805 – 817.

[38] H. Thapliyal, N. Ranganathan: Design of Efficient Reversible Logic-Based Binary and BCD Adder Circuits, ACM Journal on Emerging Technologies in Computing Systems, Vol. 9, No. 3, September 2013, pp. 17:1 – 17:31.

[39] H. G. Rangaraju, U. Venugopal, K. N. Muralidhara, K. B. Raja: Low Power Reversible Parallel Binary Adder/Subtractor, International Journal of VLSI Design & Communication Systems (VLSICS), Vol. 1, No. 3, September 2010, pp. 23 – 34.

[40] M. Shamsujjoha, F. Hossain, M. N. Y. Ali, H. M. H. Babu: Optimized Fault Tolerant Designs of the Reversible Barrel Shifters Using Low Power MOS Transistors, Journal of Computational Electronics, Vol. 14, No. 3, June 2015, pp. 726 – 746.

[41] N. Tara, H. M. H. Babu: Synthesis of Reversible PLA Using Products Sharing, Journal of Computational Electronics, Vol. 15, No. 2, June 2016, pp. 420 – 428.

[42] N. K. Misra, B. Sen, S. Wairya: Towards Designing Efficient Reversible Binary Code Converters and a Dual-Rail Checker for Emerging Nanocircuits, Journal of Computational Electronics, Vol. 16, No. 2, February 2017, pp. 442 – 458.

[43] A. Naghibzadeh, M. Houshmand: Design and Simulation of a Reversible ALU by Using QCA Cells with the Aim of Improving Evaluation Parameters, Journal of Computational Electronics, Vol. 16, No. 3, June 2017, pp. 883 – 895.

[44] M. Kianpour, R. Sabbaghi-Nadooshan: Novel 8-bit Reversible Full Adder/Subtractor Using a QCA Reversible Gate, Journal of Computational Electronics, Vol. 16, No. 2, February 2017, pp. 459 – 472.

[45] M. H. A. Khan, M. A. Perkowski: Quantum Ternary Parallel Adder/Subtractor with Partially-Look-Ahead Carry, Journal of Systems Architecture, Vol. 53, No. 7, July 2007, pp. 453 – 464.

[46] K. Ghosh, M. M. Haque, S. Chakraborty: Design of Reversible Ternary Adder/Subtractor and Encoder/Priority Encoder Circuits, Proceedings of the International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, India, April 2016, pp. 1290 – 1295.

[47] K. P. Raj, Y. Syamala: Transistor Level Implementation of Digital Reversible Circuits, International Journal of VLSI Design & Communication Systems, Vol. 5, No. 6, December 2014, pp. 43 – 61.

[48] L. O. Chua, P.- M. Lin: Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques, 1st Edition, Prentice Hall, New Jersey, 1975.

[49] M. Rahmati, M. Houshmand, M. H. Kaffashian: Novel Designs of a Carry/Borrow Look-Ahead Adder/Subtractor Using Reversible Gates, Journal of Computational Electronics, Vol. 16, No. 3, July 2017, pp. 856 – 866.

[50] M. Krumm, M. P. Müller: Quantum Computation is the Unique Reversible Circuit Model for Which Bits are Balls, Nature Partner Journals Quantum Information, January 2019, Vol. 5, No. 1, pp. 1 – 8.

[51] S. M. Saeed, N. Mahendran, A. Zulehner, R. Wille, R. Karri: Identification of Synthesis Approaches for IP/IC Piracy of Reversible Circuits, ACM Journal on Emerging Technologies in Computing Systems, Vol. 15, No. 3, April 2019, pp. 23:1 – 23:17.

[52] F. Holik, G. Sergioli, H. Freytes, A. Plastino: Logical Structures Underlying Quantum Computing, Entropy, Vol. 21, No. 1, January 2019, pp. 1 – 13.

[53] L. Gyongyosi, S. Imre: A Survey on Quantum Computing Technology, Computer Science Review, Vol. 31, February 2019, pp. 51 – 71.