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A 167.18 ppm/°C Temperature Coefficient, Area Efficient Voltage Reference Using Only MOS Transistors

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Abstract: In this paper, design of a voltage reference circuit using only MOS transistors and without employing an operational amplifier is presented. A proportional to absolute temperature [PTAT] voltage and a PTAT current are designed then difference of the PTAT voltage and product of the PTAT current and resistor gives the temperature independent voltage. The advantages of both sub-threshold and strong inversion region operation of MOS transistors are exploited in the design. The voltage reference is implemented using standard CMOS 180 nm technology. The voltage reference provides a voltage of 224.3 mV consuming a quiescent current of 30 μA at room temperature. Post layout simulation results show that the proposed voltage reference has a temperature coefficient of 167.18 ppm/°C and varies only 3mV when there is a ±10% variation in supply voltage. The circuit occupies an area of only 93.6×32.6μm on the chip, making it suitable for area constraint applications.

Keywords: Band-gap reference, Sub 1V voltage reference, PTAT, Temperature coefficient.

1 Introduction

Voltage references are vital building blocks of power management circuits and data converters. The performance metrics of above mentioned blocks rely on the accuracy of reference voltage. Voltage reference is one which produces a constant stable voltage irrespective of variations in temperature and supply voltage. It differs from voltage regulators in the fact that the latter has current driving capability. All electronic devices exhibit temperature dependency, voltage across them either increases or decreases with the increase in temperature. PTAT devices have positive temperature coefficient where as complementary to absolute temperature [CTAT] devices have negative temperature coefficient. It was Widlar [1] who showed a temperature independent device could be designed by adding PTAT and CTAT voltages

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with appropriate coefficients. The obtained voltage was 1.2 V which was known as Band-gap reference. Diode was used for generating PTAT voltage and diodes in parallel were used for generating CTAT voltage. However with the advancement in technology, reference voltage 1.2V was huge. The authors of [2, 3] proposed voltage reference circuits using parasitic BJTs which could produce sub 1 V reference voltage. Instead of adding PTAT and CTAT voltages, currents were used to produce reference voltage. But parasitic BJTs are not well characterized in standard CMOS technologies. They occupy large area and suffer from substrate current leakage problem. In the last decade, there have been many works [4 – 14] in realizing a voltage reference without using parasitic BJTs. In [15], author utilized MOSFETs operating in sub-threshold region which would behave similarly to that of BJT. In [16], a modified beta multiplier was used to generate a PTAT current and V_{GS} of MOSFET was used to produce a CTAT voltage. Later using V to I converter, CTAT current was generated. However large resistors were used occupying large area on the chip. A weighted V_{GS} MOS architecture with bulk bias was utilized for the generating CTAT voltage and PTAT voltage in [17]. But it was susceptible to process variations. The author of [18] proposed a PVT compensated sub-micro ampere current reference. The inverse process dependency between intrinsic trans-conductance and the threshold voltage of the MOS transistor at any process corner was utilized to achieve better robustness. Though the circuit consumed very less current, the obtained temperature coefficient was poor. In [19], a voltage reference was implemented using only MOS transistors and experimentally validated the operation. However the structure required two op-amps and produced voltage was not sub 1V. In the present paper, a voltage reference which is devoid of operational amplifier, parasitic BJTs and large resistors is proposed. Section 2 describes the design and working principle of voltage reference. The simulation results and discussion are presented in Section 3. In the final section the conclusion derived from results are given.

2 Methodology

Voltage references without using parasitic BJTs depend on MOSFET threshold voltage [V_{TH}], electron mobility [μ_n], thermal voltage [V_T] and sub-threshold region of operation to produce PTAT and CTAT voltages [4].

Temperature dependency of threshold voltage, mobility and thermal voltage can be given by

$$V_{TH} = V_{TH0} - kT\,, \tag{1}$$

$$\mu(T) = \mu(T_0)(T/T_0)^{-m}\,, \tag{2}$$

$$v_T = \frac{k_B T}{q}\,, \tag{3}$$

where, $\mu(T_0)$ is the carrier mobility at room temperature T_0, m is the mobility temperature exponent, V_{TH0} is the threshold voltage at 0°K, k is the temperature coefficient of V_{TH}, k_B is Boltzmann's constant, q is electron charge.

Equations (1), (2) and (3) reveal that threshold voltage and carrier mobility have negative temperature coefficients whereas thermal voltage has positive temperature coefficient. The behavior of MOSFET in sub-threshold region can be approximated to that of BJT. Drain current I_D exhibits an exponential relationship with V_{GS} as shown in (4).

$$I_D = I_0 (W/L) \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T} \right) \tag{4}$$

where $I_0 = \mu_n C_{OX} (\eta - 1)^2$, V_{TH} is the threshold voltage of NMOS, η is the sub threshold slope factor, μ is the carrier mobility. V_T is the thermal voltage, C_{OX} is the gate oxide capacitance. The core structure of proposed voltage reference is shown in Fig. 1.

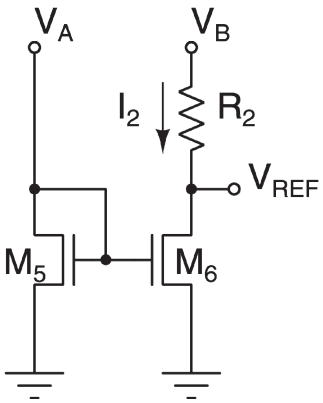


Fig. 1 – *Basis of proposed voltage reference.*

If V_A and V_B both voltages are PTAT voltages and $V_A = V_B$, then

$$V_{REF} = V_B - I_2 R_2 = V_{PTAT} - I_{PTAT} R_2 \ . \tag{5}$$

Hence by using proper value of R_2, V_{REF} can be made a temperature independent voltage.

PTAT nature of V_A and V_B can be obtained from V_{GS1} of the circuit shown in Fig. 2.

All MOSFETs are operating in strong inversion region.

$$V_{GS1} = V_{GS2} + I_1 R_1 \ , \tag{6}$$

$$I_1 = \frac{2}{R_1^2 \mu_n C_{OX} (W/L)_1} \left(1 - \frac{1}{\sqrt{K}}\right)^2 , \tag{7}$$

$$(W/L)_1 = K(W/L)_2 .$$

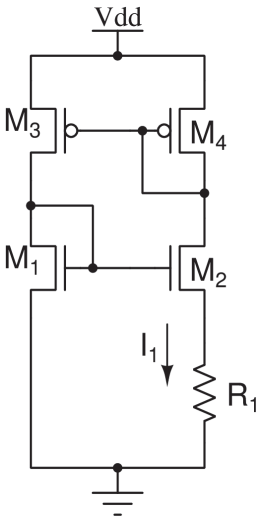


Fig. 2 – *PTAT voltage generator*.

From equation (7), I_1 has a positive temperature coefficient. In equation (6),

$$V_{GS1} = V_{CTAT} + I_{PTAT} R_1 . \tag{8}$$

By adjusting I_{PTAT} and R_1 values, V_{GS1} can be made a PTAT voltage. To make V_A equals to V_B, bootstrap current mirror is used. Fig. 3 shows the complete circuit diagram of proposed voltage reference. A start-up circuit is added so that zero biasing current condition is avoided.

When temperature increases, V_{GS1} of M_1 also increases. Since supply voltage of reference circuit is derived from this V_{GS1}, the values of V_{GS5}, V_B and I_2 increase. From (5) by using proper resistance R_2, V_{REF} can be made independent of temperature variation.

The voltage produced by proposed voltage reference is constant though there are any variations in the supply voltage. PTAT generator stage also does the task of per-regulation. Equation (7) shows that I_1 is independent of V_{DD} ignoring channel length modulation. In the final stage due to negative feedback, V_{REF} is maintained at constant value. A capacitor of 2pF capacitance is connected at the output of the PTAT generator stage for the stability purpose. **Table 1** shows the device parameter values of voltage reference circuit.

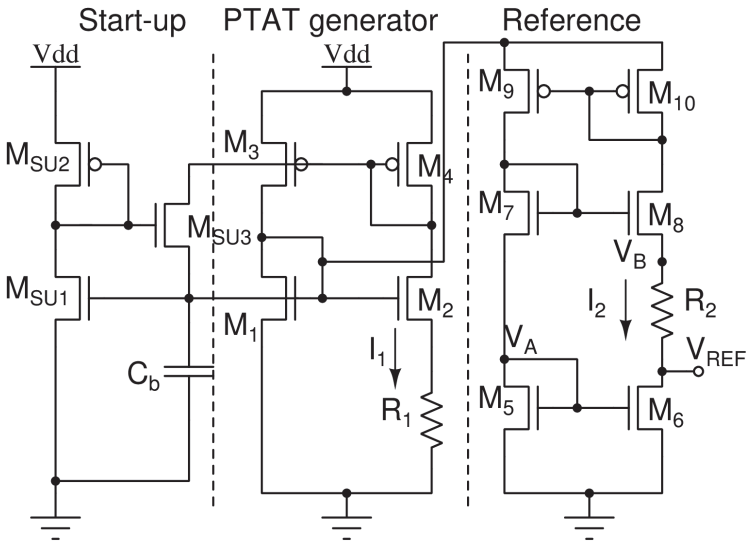


Fig. 3 – *Complete circuit diagram of proposed voltage reference.*

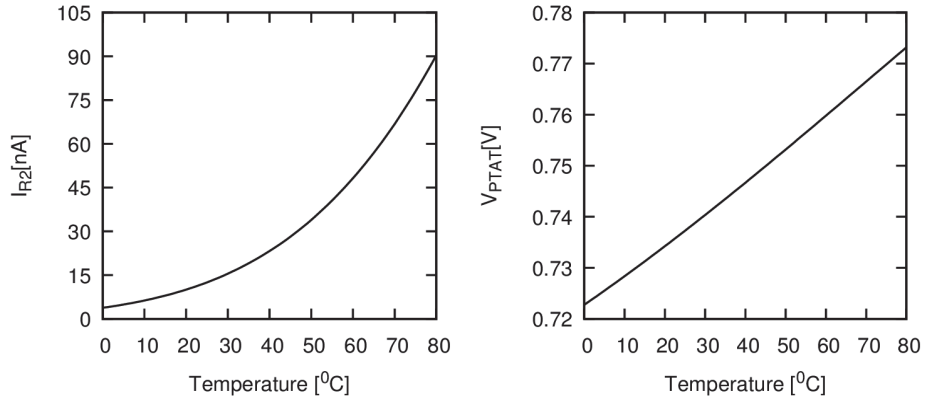
Table 1
Device parameters values.

DEVICE	PARAMETER	VALUES
M_1, M_2	W/L	1 µm/1 µm
M_3, M_4	W/L	2 µm/1µm
M_5, M_6, M_7, M_8	W/L	20 µm/1 µm
M_9, M_{10}	W/L	40 µm/1 µm
M_{SU1}	W/L	5 µm/1 µm
M_{SU2}	W/L	1 µm/5 µm
M_{SU3}	W/L	10 µm/1 µm
R_1	Resistance	12 kΩ
R_2	Resistance	110 kΩ
C_b	Capacitance	2 pF

3 Results and Discussion

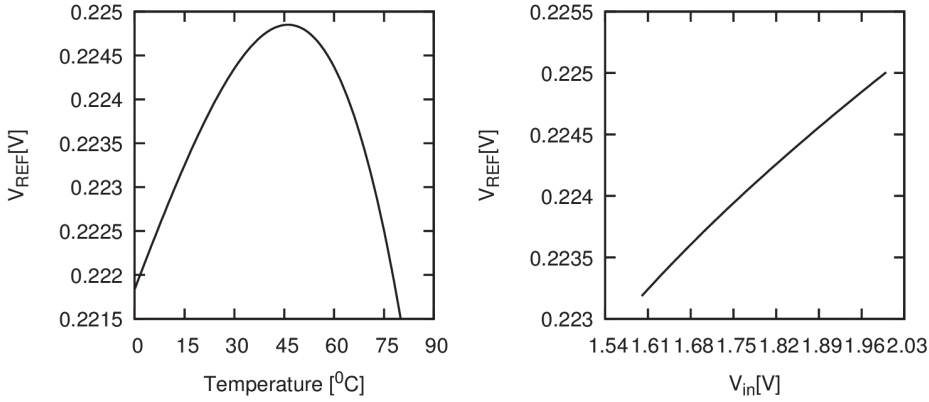
The proposed voltage reference circuit was designed and laid out in 180 nm standard CMOS technology and BSIM3v3 spice model parameters were used for simulation. Post layout simulation results after the parasitic extraction are elaborated in this section. Hence all the results include the effect of parasitic capacitances and related non-linearity. PTAT response of I_{R2} current and source voltage [V_{GS1}] of reference circuit are shown in Fig. 4a and Fig. 4b, respectively. The response of reference voltage against temperature variation from 0°C to 80°C is shown in Fig. 5a.

The recorded temperature coefficient was 167.18 ppm/°C.



(a) (b)

Fig. 4 – (a) *PTAT response of I_{R2} current;*
(b) *PTAT response of source voltage.*



(a) (b)

Fig. 5 – (a) *Temperature response of voltage reference;*
(b) *Supply response of voltage response.*

When there was ±10% variation in power supply, the reference voltage varied only 2.8 mV from the nominal value as shown in Fig. 5b. The supply was changed from 0V to 1.8V after a delay to verify whether the circuit would latch on to zero bias current or not. Due to start-up circuit, voltage reference was able to overcome zero bias current latch problem as shown in Fig. 6a.

The voltage reference exhibited an excellent power supply rejection response as shown in Fig. 6b. The measured PSRR at 100 kHz was 54 dB.

To investigate the effect of process variations on the proposed voltage reference circuit, line regulation and temperature response were tested under

three process corners namely, typical (tt), slow(ss) and fast (ff). The performance was satisfactory as shown in Figs. 7a and 7b respectively.

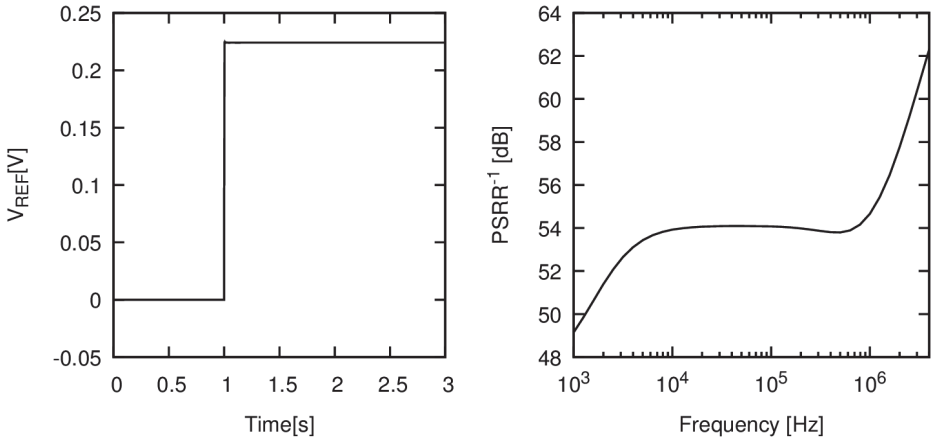


Fig. 6 – (a) *Transient response of voltage reference;*
(b) *PSRR response of voltage reference.*

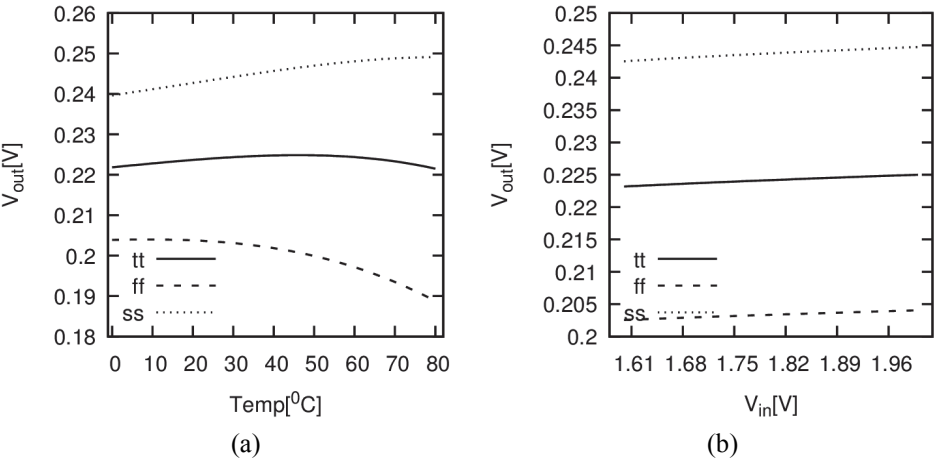


Fig. 7 – (a) *Temperature response at different process corner*s;
(b) *Supply response at different process corners.*

The layout picture of proposed voltage reference circuit is depicted in Fig. 8. The circuit occupied 93.6×32.6 μm area on the chip. To determine the operation of proposed voltage reference circuit under nonidealities like parasitic impedance, process variation Monte-Carlo statistical simulation was carried out.

The threshold voltage and carrier mobility are the major process parameters which are usually effected by nonidealities.

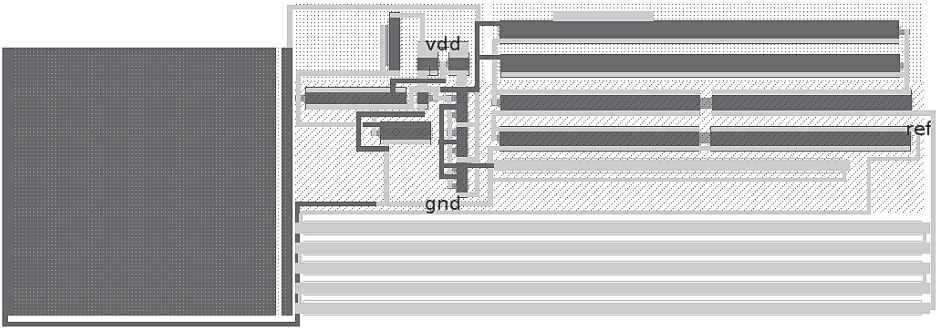


Fig. 8 – *Layout of the voltage reference.*

Assuming Gaussian probability distribution for the variation, reference voltage for different samples are plotted in Fig. 9a. Similarly one more Monte-Carlo analysis was carried out to determine the effect of nonidealities on temperature coefficient. Fig. 9b shows the histogram plot of temperature coefficient for different samples. In the both cases peak occurs at nominal value which proves the proposed voltage reference is robust.

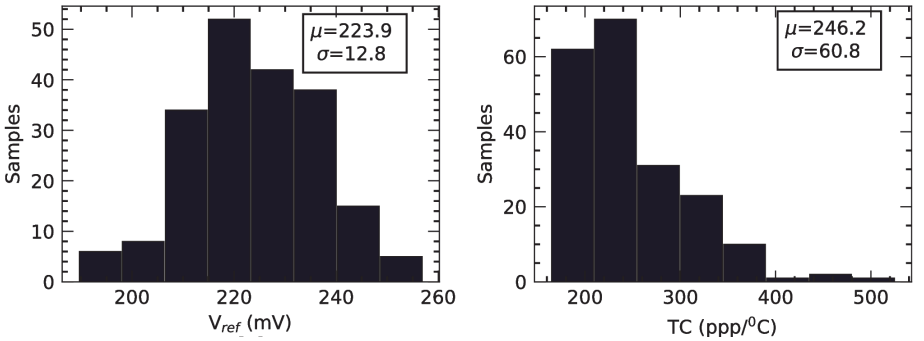


Fig. 9 – (a) *Histogram plot of reference voltage for different samples;*
(b) *Histogram plot of TC for different samples.*

Table 2 shows the performance comparison of proposed voltage reference with the recent works. It is evident from that table that proposed voltage reference has a good temperature coefficient. Though the voltage reference of [9, 12 – 13] have lesser temperature coefficients, the proposed voltage reference has the better PSRR performance.

Table 2
Performance comparison with other voltage references.

Parameters	[4]	[9]	[10]	[11]	[12]	[13]	[14]	**This work**
Technology[nm]	180	350	90	32	180	180	65	**180**
V_{DD} **[V]**	0.85	1.5	1.2	0.9	1.4	0.4	0.4	**1.8**
V_{REF} **[mV]**	221	1038	115	550	1.25	210	0.34	**224.4**
I_Q **[µA]**	3	0.3	--	--	--	--	--	**30**
Temp. coefft. [ppm/°C]	271	87	518	962	73	82	252	**167.18**
PSRR [dB]	--	49	31	--	41	47	--	**54**

4 Conclusion

In this paper, the design of a voltage reference without using operational amplifier, parasitic BJTs and large resistors is demonstrated. PTAT voltage and PTAT current derived from MOSFETs operating sub-threshold region are used to produce a temperature independent voltage. The proposed voltage reference is laid out in standard 180 nm CMOS technology and occupies a very small area on the chip. The post layout results show that the voltage reference has better temperature coefficient and PSRR response.

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