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Benchmarking of Phase Lock Loop Based Synchronization Algorithms for Grid-Tied Inverter

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Abstract: In renewable energy-based generation sources a phase locked loop is one of the most popular synchronization techniques. A rapid and precise grid voltage phase and frequency estimation under a wide spectrum of possible grid disturbances is its main objective. This paper compares popular grid synchronization algorithms on grid voltage anomalies. The compared algorithms are divided in three groups: without filtering, with filtering in synchronous reference frame and with filtering in stationary reference frame. The behaviour of the algorithms is tested in a laboratory, using dSpace 1103 as a platform on which the algorithms are compiled and OMICRON CMC 356 as a programmable grid voltage generator. The benchmarks conducted in this paper include voltage sags, grid voltages harmonics, DC offset and frequency step change. The obtained results show that there are significant differences in tested PLL responses for some networks disturbances.

Keywords: Benchmarking, Grid synchronization, Phase locked loop, Grid disturbance.

1 Introduction

Renewable energy-based generation sources enabled the use of power electronics devices as an interface bridge between DC or variable frequency AC supply and the main power grid or local loads. Power electronic inverters in various topologies represent the interface with the main goal of extracting and delivering the maximum high-quality power from renewable energy sources. A two level, three-phase pulse width modulated voltage source inverter (VSI) is the most common option for low and medium power applications.

The interaction of renewable energy sources over the invertor with the main grid or between several inverters are accompanied with the process called synchronization [1 – 3]. To obtain the grid synchronization between the main grid voltages and the inverter output voltages in the Point of Common Coupling

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(PCC), it is necessary to have precise information of the grid voltage fundamental component magnitude, phase and frequency. Basically this information is important for safe and reliable work of inverters in parallel with the main grid or among them in isolated grid and the monitoring of the grid conditions [4].

The Phase Lock Loop (PLL) algorithms are most commonly used to estimate the phase and frequency of the main grid voltage. They belong to the group of closed-loop synchronization algorithms, which use a feedback of one or more signals in the control structure. First PLL techniques have been used in telecommunications since 1930s, and they have been adopted in many technical fields since then, one of them being the control of grid connected inverters. In general a PLL with low gain is used here compared with high gain ones in telecommunications. The reason for this is a tradeoff between disturbance rejection capability and tracking speed due to the voltage distortion in the main grid. In general, all synchronization techniques provide satisfactory results in laboratory conditions with the grid voltage free of the noise and disturbances. In real grid the power quality is considered an important precondition for regular operation of the PLL structure. Different factors in the grid could cause a presence of harmonics, interharmonics, voltage sags, swells, imbalances and DC offset in real or measured voltages [5, 6]. All these occurrences affect the tracking capability of PLL for precise fundamental grid voltage phase angle [7, 8]. This is the main reason for continuous development and improvement of the existing PLL techniques in order to achieve reliable operation with better stability and faster synchronization for a large number of grid voltage disturbances without large computational overhead.

The aim of this paper is to present the overview and comparison between popular PLL algorithms for grid connected inverters as in [9]. The algorithms selected for comparison can be grouped in three categories, without grid voltage filters, with filters in synchronous reference frame (*dq*), and with filters in stationary reference frame (αβ). For the first category, Synchronous Reference Frame (SRF) and Decoupled Double Synchronous Reference Frame (DDSRF)-PLLs are selected [10, 11]. In the second category two (*dq*) reference frame filters are compared, namely Moving Average Filter (MAF) and its improved Enhanced version with Pre-filtering stage (EPMAF Type 2) both with SRF-PLL for grid voltage phase angle estimation [12, 13]. Grid voltage filter in the third category consists of Dual Second-Order Generalized Integrator (DSOGI) placed in (αβ) reference frame and synchronization is achieved in combination with SRF-PLL [14]. The behavior of the selected algorithms is observed and compared in conditions of voltage sags, harmonics and DC offset. Synchronization algorithms are created in MATLAB/Simulink, compiled to dSpace 1103 board and executed in parallel with sampling time of 100 μs. Grid voltages with mentioned disturbances are recreated using Omicron 356 and fed into dSpace through voltage sensors.

The rest of the paper is organized as follows. A short basic description of popular grid synchronization algorithms along with their block diagrams and small signal models is provided in Section 2. Section 3 describes devices used in experimental setup and tests that the algorithms are subjected to. The behaviour of the described algorithms is shown and discussed in Section 4. Finally, the paper ends with some conclusions and references.

2 Review of Popular Three-Phase PLL Techniques

Conventional PLL structures consist of three basic elements: a phase detector (PD) for signal generation with the phase error information, a loop filter (LF) for phase error elimination, and a frequency/phase generation block also called voltage-controlled oscillator (VCO).

2.1 SRF-PLL algorithm

One of the simplest PLL algorithms is SRF-PLL illustrated in Fig. 1. It uses Clarke's and Park's transformation to transfer three-phase grid voltage vector from *abc* to *dq* domain. Assuming that the grid instantaneous voltages are symmetrical and pure sinusoidal, they can be written as (1):

$$\begin{aligned} V_a &= V_m \cos \omega t \\ V_b &= V_m \cos\left(\omega t - \frac{2\pi}{3}\right), \\ V_c &= V_m \cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

where V_m denotes maximum amplitude of phase voltage and ωt actual grid voltage phase angle. Instantaneous voltages in synchronous reference frame can be obtained according to:

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3}\left[T_{dq}\right]\left[T_{\alpha\beta}\right]\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \tag{2}$$

using following Clarke's $T_{\alpha\beta}$ (3) and Park's T_{dq} (4) transformation:

$$\left[T_{\alpha\beta}\right] = \frac{2}{3}\begin{bmatrix} 1 & \cos\left(\frac{2\pi}{3}\right) & \cos\left(\frac{4\pi}{3}\right) \\ 0 & \sin\left(\frac{2\pi}{3}\right) & \sin\left(\frac{4\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}, \tag{3}$$

$$\left[T_{dq}\right]=\begin{bmatrix}\cos\theta & \sin\theta & 0\\ -\sin\theta & \cos\theta & 0\\ 0 & 0 & 1\end{bmatrix}. \tag{4}$$

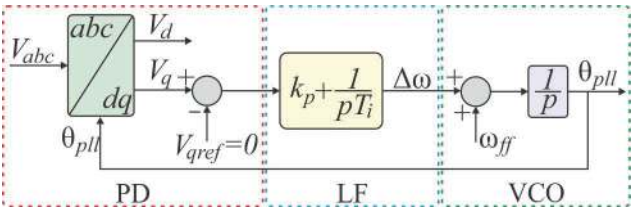

Fig. 1 – *Block diagram of the SRF-PLL.*

The angle between the grid voltage vector and *d*-axis of synchronous reference frame is denoted as θ. Using trigonometric identities, direct transformation from *abc* to *dq* domain can be derived as:

$$\begin{bmatrix}v_d\\ v_q\\ 0\end{bmatrix}=\begin{bmatrix}\cos(\omega t-\theta)\\ \sin(\omega t-\theta)\\ 0\end{bmatrix}V_m. \tag{5}$$

With SRF-PLL angular position of *dq* rotating frame is controlled by the feedback loop. For small angle differences (between ω*t* and θ), a term $V_m\sin(\omega t-\theta)$ can be approximated as $V_m(\omega t-\theta)$. In the case of the ideal grid voltage vector alignment with the d component, q component of grid voltage is zero. Bandwidth of SRF-PLL's control loop can be high, yielding a fast and precise grid phase angle detection, if grid voltage is without either unbalance or harmonics [11]. In case of distorted grid voltage with higher order harmonics, the bandwidth of the control loop has to be reduced. The most commonly used LF is the PI controller, and since it behaves as a first order low pass filter, it does not represent an effective solution for disturbance rejection of dominant higher harmonics in low voltage grid [16]. A small signal model of SRF-PLL is shown in Fig. 2.

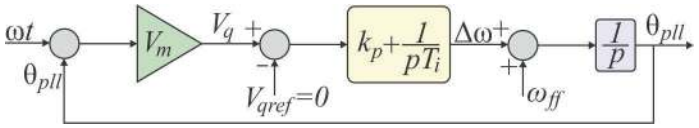

Fig. 2 – *Block diagram of the SRF-PLL small signal model.*

Using the small signal model, linear second order transfer function can be obtained (6). Comparing this second order closed loop transfer function with the

canonical second-order transfer function (7) which has two poles and one zero, a proportional k_p and integral T_i term can be calculated using pole zero placement method, by selecting natural frequency ω_n and damping ratio ζ, with comparison of appropriate coefficients:

$$G_{cl}(p) = \frac{\theta_{pll}(p)}{\omega t(p)} = \frac{V_m k_p p + V_m \frac{1}{T_i}}{p^2 + V_m k_p p + V_m \frac{1}{T_i}}, \tag{6}$$

$$G_{cf}(p) = \frac{2\zeta\omega_n p + \omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}. \tag{7}$$

In previous equation, p denotes Laplace complex variable. On the basis of comparison (6) and (7), expressions for k_p (8) and T_i (9) are obtained:

$$k_p = \frac{2\zeta\omega_n}{V_m}, \tag{8}$$

$$T_i = \frac{V_m}{\omega_n^2}. \tag{9}$$

2.2 DDSRF-PLL algorithm

The real three-phase grid conditions mostly deviate from the assumption of the grid voltages and currents symmetry. In this case it is necessary to reduce the bandwidth of the SRF-PLL structure, resulting with precise but slow synchronisation. The connection of the distributed energy sources to the power grid and their resynchronization due to grid failures requires a quick response of the synchronization unit, which is not possible with the SRF-PLL algorithm under the above mentioned conditions. The appearance of voltage asymmetry is especially interesting, not only for estimation of angle and frequency but also for estimating the amplitude of the grid voltage components in *dq* synchronous reference frame. The amplitude of the voltage components is used in the control algorithm, so their exact value is crucial for the reliable control of the distributed power source. In the context of symmetrical components, an unbalanced three phase system can be expressed as a sum of three symmetrical systems, one rotating in the same direction as the system under study (direct), other rotating in the opposite direction (inverse) and the third with phasors in phase with each other (zero). For three phase grid synchronization, any deviation from the symmetrical system results in inverse sequence occurrence. From the standpoint of direct sequence system, inverse system rotates with twofold fundamental frequency. In SRF-PLL this results in occurrence of harmonic close to the fundamental frequency that cannot be successfully suppressed by LF. All of this conditioned need to improve the basic SRF-PLL

in order to overcome the mentioned problems. Due to the inverse component, the use of two reference systems, direct and inverse is necessary. The algorithm that expresses grid voltage vector through its direct and inverse sequence components using double synchronous reference frame is called Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) [11] and its block diagram is presented in Fig. 3.

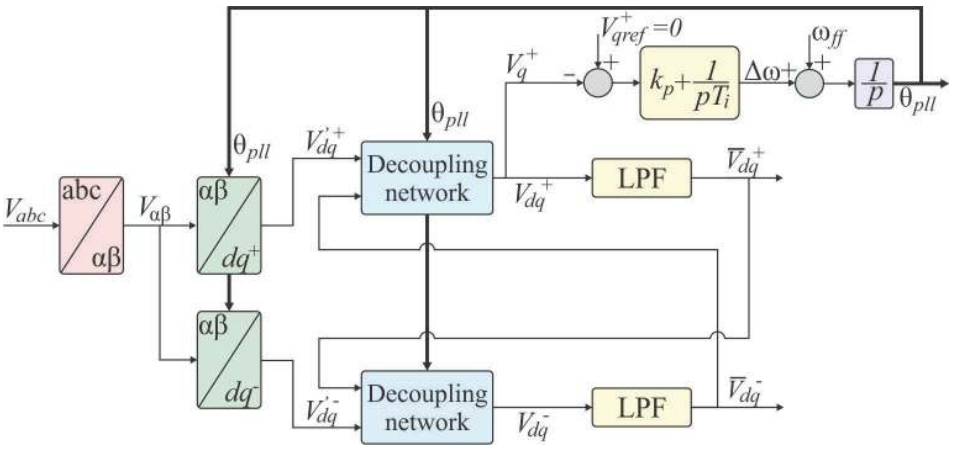

Fig. 3 – *Block diagram of the DDSRF-PLL.*

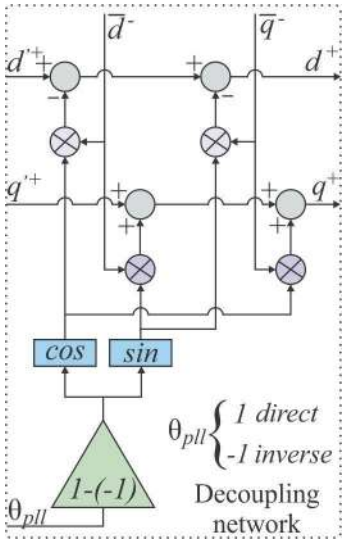

Fig. 4 – *Block diagram of the decoupling network (adopted from [14]).*

For an extraction of direct sequence grid voltage vector, cross-feedback decoupling network is needed along with the Low Pass Filter (LPF). LPF block is usually selected with first order transfer function presented in (10):

$$LPF(p) = \frac{\omega_f}{p + \omega_f}, \tag{10}$$

where ω_f presents LPF's cut-off frequency. For a stable response of the PLL, ratio of cut-off frequency and fundamental grid frequency has to be less than 0.707 ($\omega_f / \omega < 1/\sqrt{2}$) [11]. An illustration of decoupling network for direct sequence is shown in Fig. 4.

2.3 MAF-PLL algorithm

Different filtering techniques are popular methods for overcoming the challenge of precise phase and frequency estimation for various conditions of grid voltages. Due to its simple digital realization, low computational burden and effectiveness, moving average filter (MAF) is one of the most widely used techniques today [12]. MAF is a linear phase finite impulse response (FIR) filter. It can act as an ideal LPF if certain conditions are met [19].

Continuous time domain description of MAF with the input signal *x(t)* and the output signal $\bar{x}(t)$ is:

$$\bar{x}(t) = \frac{1}{T_W} \int_{t-T_W}^{t} x(\tau)\, d\tau, \tag{11}$$

where T_W is MAF's window length. In complex domain, after Laplace transformation, MAF transfer function is:

$$F_{MAF}(p) = \frac{1}{T_W} \frac{1 - e^{-T_W p}}{p}. \tag{12}$$

Linearized model of MAF can be obtained using first order Padé approximation:

$$F_{MAF}(p) = \frac{1}{1 + \frac{T_W}{2} p}. \tag{13}$$

The implementation of (11) in *z*-domain has the form given in (14) where N represents MAF window length. A block diagram of MAF realisation in discrete time domain is presented in Fig. 5. Finally, implementation of MAF in combination with SRF-PLL is shown in Fig. 6.

$$F_{MAF}(Z) = \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}}. \tag{14}$$

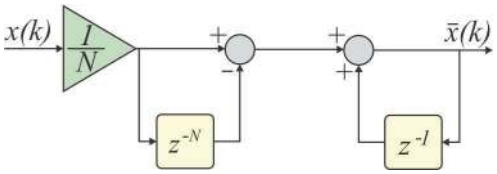

Fig. 5 – *MAF realization in z domain.*

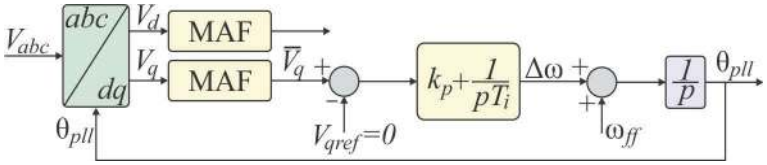

Fig. 6 – *Block diagram of the MAF-PLL.*

The main advantage of MAF-PLL over traditional SRF-PLL is its harmonic rejection capability. Considering harmonic limits defined by various standards, for three phase grid tie inverters odd harmonics non-multiples of 3 (5th, 7th and 11th) present the biggest challenge for synchronization. When transferred in *dq* synchronous rotating system, different harmonics have different frequencies, depending on the fact whether the harmonic of interest has positive or negative sequence. All the previously mentioned characteristic harmonics are even and with frequencies as whole-number multiplies of 100 Hz after *dq* transformation. The window length of MAF that corresponds to 10 ms timespan (100 Hz) will successfully cancel out these harmonics.

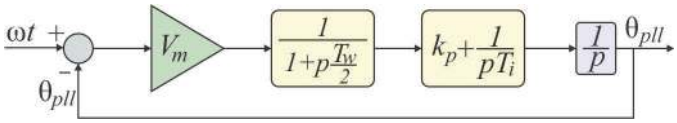

Fig. 7 – *Small signal model of the MAF PLL.*

Parameters tuning of PI-controller inside MAF-PLL can be made with small signal model of MAF-PLL as shown in Fig. 7. Open loop transfer function derived from small signal model has a form:

$$G_{ol}(p) = \frac{pV_m T_i k_p + V_m}{p^3 T_i \frac{T_W}{2} + p^2 T_i + pV_m T_i k_p + V_m}. \tag{15}$$

PI controller parameters calculations using symmetrical optimum method provide proportional gain (16) and integral time constant (17):

$$k_p = \frac{1}{V_m T_W}, \tag{16}$$

$$T_i = 2V_m T_W^2 . \tag{17}$$

According to the recommendations from [12], small modification of proportional gain and integral time is introduced in (18) and (19):

$$k_p = \frac{2}{V_m b T_W}, \tag{18}$$

$$T_i = \frac{V_m b^3 T_W^2}{4} . \tag{19}$$

The value for constant b is 2.4 according to [12] in order to make transient response fast and well-damped.

2.4 EPMAF-PLL type 2 algorithm

The main drawback of classical MAF-PLL is slow dynamic response and phase error under off-nominal grid frequency [13]. Moving MAF filter before *dq* transformation (Pre-filtering stage) leads to improved dynamic and straightforward controller tuning procedure (PMAF-PLL). Enhanced response under offset error was the next iteration (EPMAF-PLL), although it suffered from high frequency overshoot at the time of fault and inaccurate harmonic compensation in cases of off-nominal grid frequency [14]. Modification of pre-filtering stage in EPMAF-PLL yields performance improvement in all previously mentioned cases and reduction of offset error and MAF with these modifications is called EPMAF-PLL type 2, which block diagram is shown in Fig. 8.

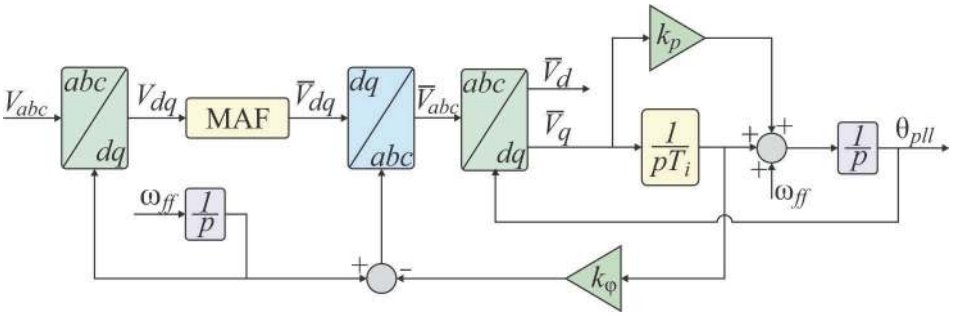

Fig. 8 – *Block diagram of the EPMAF-PLL (type 2).*

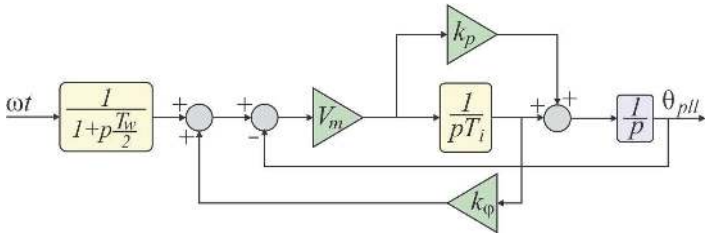

Fig. 9 – *Small signal model of the EPMAF-PLL type 2.*

Small signal model of EPMAF-PLL type 2 is shown in Fig. 9.

According to the small signal model, closed loop transfer function can be obtained as:

$$G_{cl}(p)=\frac{\theta_{pll}(p)}{\omega t_{maf}(p)}=\frac{V_m k_p p+V_m\dfrac{1}{T_i}}{p^2+pV_m\left(k_p-\dfrac{k_\varphi}{T_i}\right)+V_m\dfrac{1}{T_i}}. \tag{20}$$

The system is stable, by Routh Hurwitz criterion, under condition $0<k_\varphi/T_i<k_p$. Taking into account this consideration, transfer function is second order system and parameters of regulator can be tuned according to desired dynamic. Proportional gain and integral time of PI controller are:

$$k_p=\frac{\omega_n}{V_m}\left(2\zeta+k_\varphi\omega_n\right), \tag{21}$$

$$T_i=\frac{V_m}{\omega_n^2}. \tag{22}$$

2.5 DSOGI-PLL algorithm

Unlike the previous two filtering methods, DSOGI extracts fundamental direct sequence for SRF-PLL in stationary reference frame. It utilizes a Second-Order Generalized Integrator (SOGI) to create quadrature signals. Quadrature signals can also be created using transport delay methods, but such methods are not frequency adaptive and have poor harmonic disturbance rejection. The SOGI consists of the LPF used for harmonic filtering and orthogonal signal generation, along with the Band Pass Filter (BPF) used only for harmonic filtering [15]. The block diagram of the SOGI is presented in Fig. 10.

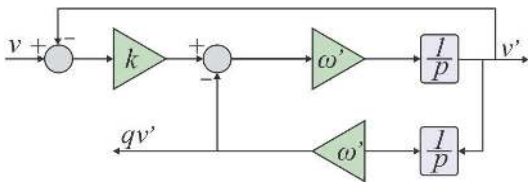

Fig. 10 – *Block diagram of the SOGI.*

In the previous scheme ω' denotes estimated frequency and k denotes a damping factor. In [14] gain k is experimentally selected to be $1/\sqrt{2}$. Transfer function of the SOGI's BPF and LPF can be derived from block diagram as:

$$BPF(p)=\frac{v'(p)}{v(p)}=\frac{k\omega p}{p^2+k\omega p+\omega^2}, \tag{23}$$

$$LPF(p)=\frac{qv'(p)}{v(p)}=\frac{k\omega^2}{p^2+k\omega p+\omega^2}. \tag{24}$$

Direct voltage sequence in stationary frame is extracted using two SOGIs along with Positive-Sequence Calculator (PSC). Block diagram of complete DSOGI-PLL is shown in Fig. 11.

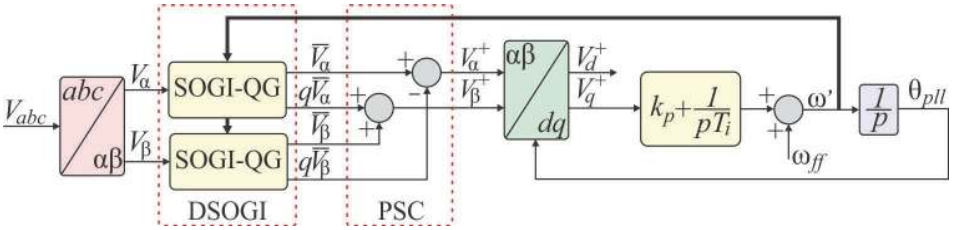

Fig. 11 – *Block diagram of the DSOGI-PLL.*

3 Experimental Design and Setup

The performance of all described synchronization algorithms was tested on the hardware/software setup in the laboratory for electric machines and drives at the Faculty of EE.

3.1 Description of experimental setup and tests

An overview of the experimental setup can be seen in Fig. 12. It consists of:

1. MATLAB/Simulink software for grid conditions simulation;
2. Omicron Test Universe for grid condition file import;
3. Omicron CMC 356 for grid voltage generation from file;
4. Voltage conditioners CA30 [17] and dSPACE connection hub;
5. dSPACE 1103 rapid prototyping board for synchronization algorithm implementation;
6. dSpace Control Desk environment for experiment verification.

All the algorithms are built using MATLAB/Simulink in digital domain and compiled on dSpace 1103 rapid prototyping platform with a sampling time of 100 μs. The algorithms work independently of one another in parallel using the same voltage measurements. MATLAB/Simulink is used to simulate various grid voltage disturbances and to transfer simulated voltage waveforms into the output file with IEEE COMTRADE format. Desired grid voltage waveforms are

generated on OMICRON's voltage outputs based on transient records loaded in appropriately formatted file. Reproduced waveforms have nominal phase voltage of 230 V and nominal frequency of 50 Hz. Outputs of all synchronization algorithms are observed and recorded using dSpace Control Desk.

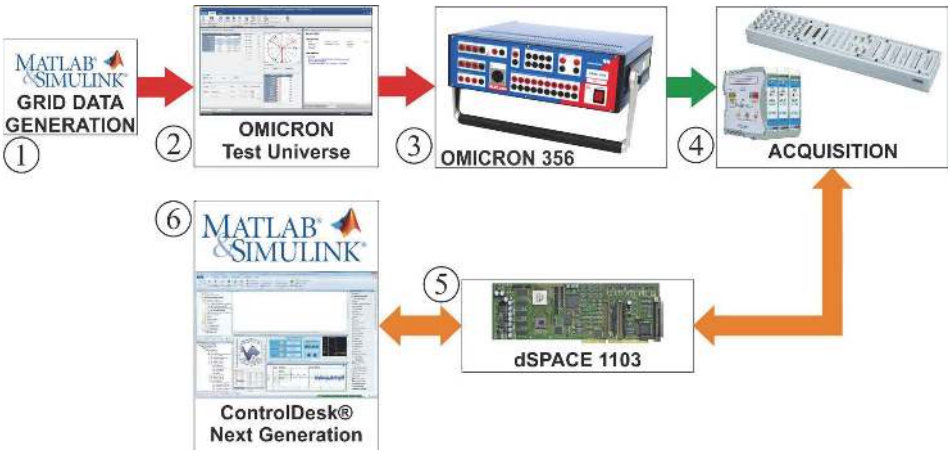

Fig. 12 – *Overview of the experimental setup.*

Since it can be expected for grid inverters in a laboratory to work in micro-grid regimes without neutral conductor, the algorithms are adopted to line to line voltage measurements using voltage sensors and mathematically transferred to phase voltage in the control algorithm.

Most grid-tied inverters today are located in low voltage grid that can operate in various regimes. The synchronization algorithms have to be tested on anomalies that can be expected in low voltage grid and on anomalies that may occur is the inverter itself has a defect. The algorithms are tested for the following scenarios:

1. Sags A to G [18];
2. Harmonics;
3. DC offset in measurement sensor;
4. Step frequency change;
5. Initial grid inverter synchronization during regular operation.

3.2 Overview of PLL algorithms parameters

For all tested algorithms, PI controller is used as a LF inside the SRF-PLL. The parameters of LF are obtained by selecting natural frequency of the system ω_n as 10 rad/s and damping ratio ζ as 0.707. Natural frequency has a slightly

lower value than typical and as a consequence the SRF-PLL will have a better filtering capability and a slower response time.

All parameters of synchronization algorithms are provided in **Table 1.**

Table 1

Parameters of synchronization algorithms.

Algorithm	Controller		Additional
	k_p	T_i	
SRF-PLL	0.2732	0.08239	/
DDSRF-PLL	0.2732	0.08239	$\omega_f = 188.5$
MAF-PLL	0.2562	0.1124	$N = 100$ $b = 2.4$
EPMAF-PLL Type 2	0.3581	0.08239	$N = 100$ $k_\varphi = 0.007$
DSOGI-PLL	0.2732	0.08239	$k = 0.707$

4 Experimental Results and Comparison

The first set of experiments included voltage sags with a 70 % residual voltage. All sags occurred 3 seconds after start of the experiment and lasted for 1 second. Transition from nominal grid voltage to sag is rectangular and at the moment when phase a cross zero. In the Figs. 13a –13c response of algorithms is shown in the case of type A to G voltage sags.

In the case of voltage sag type A, any algorithms have no problem in a steady state frequency estimation. At the moment of sag occurrence and recovery, DDSRF and DSOGI-PLLs have a short transition period in frequency estimation with a similar settling time. SRF, MAF and EPMAF-PLLs did not exhibit any deviation in frequency estimation from steady state at the time of sag. During all other sags, only SRF-PLL has an undamped oscillation at the frequency of 100 Hz. This is expected behaviour since it cannot effectively suppress inverse sequence voltage disturbances.

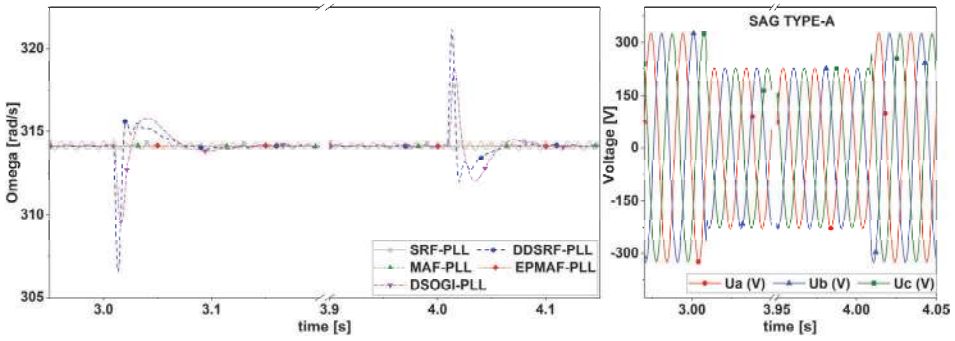

Fig. 13a – *Response of algorithms in the case of type A to G voltage sags.*

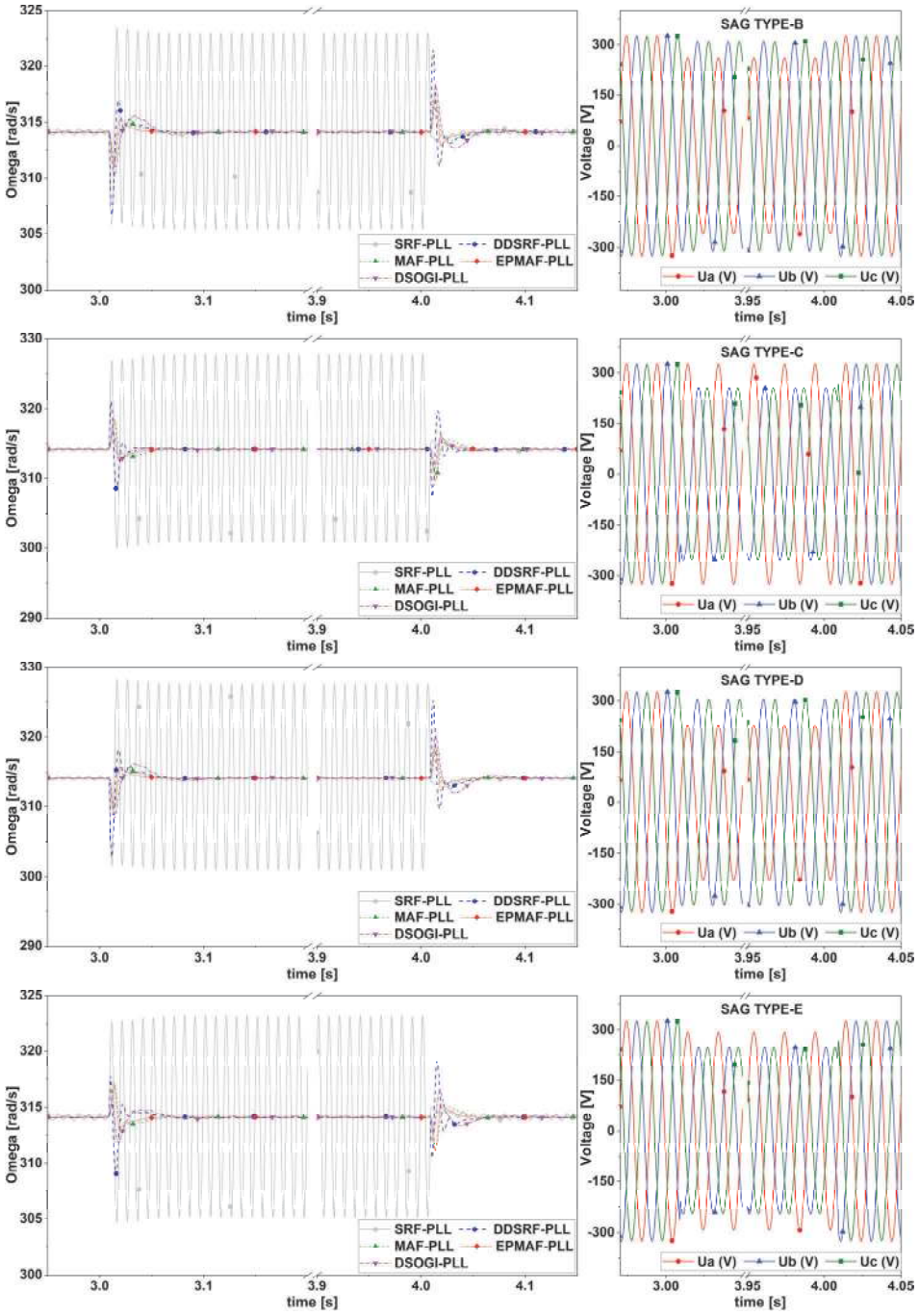

Fig. 13b – *Response of algorithms in the case of type A to G voltage sags.*

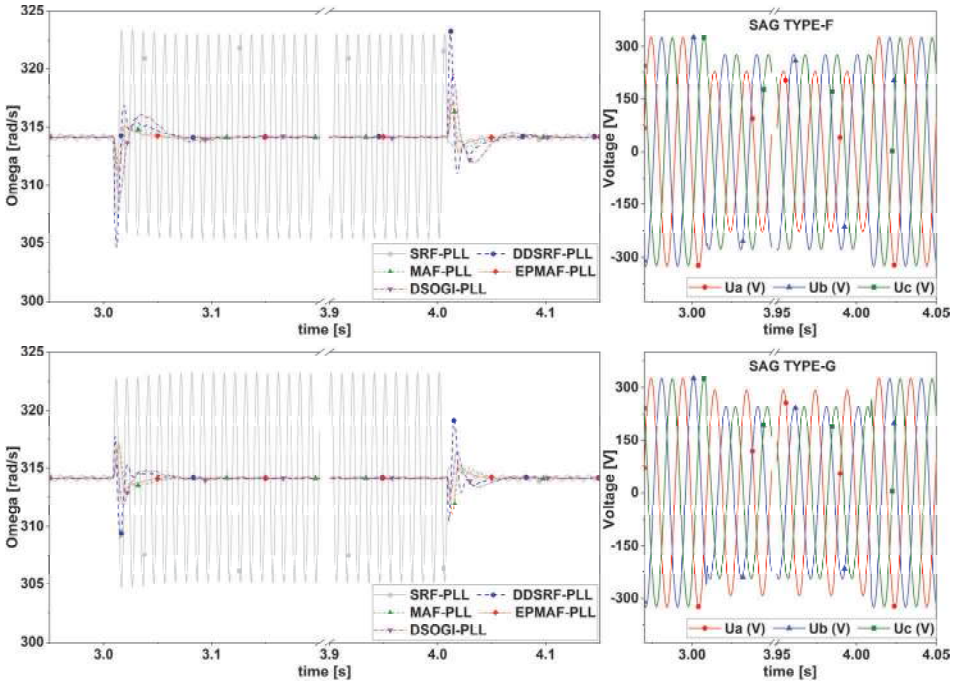

Fig. 13c – *Response of algorithms in the case of type A to G voltage sags.*

If the previous results are compared to the ones from [9], it can be concluded that all voltage sags that induce inverse voltage component result in undamped oscillations in SRF-PLL's frequency estimation.

The second test included voltage harmonics. During this test, after 3 seconds from the start, maximal allowed level of odd harmonics (according to the IEC EN 50160 standard: 6 % of 5^{th}, 5 % of 7^{th} and 3.5 % of 11^{th}) were added to the ideal grid voltages and used for testing. Results can be seen in Fig. 14.

Similar frequency estimation from SRF and DDSRF-PLL can be seen in previous figure. They cannot suppress higher harmonics effectively using only loop filter. DSOGI-PLL has undamped oscillation, but much smaller in magnitude. Both MAF and EPMAF type 2 PLL have rejected disturbances in control loop after one window length. Testing on harmonics conducted in [9] provided similar results.

Presence of DC offset is investigated in the third test. Voltage conditioner in phase "a" used for measurements in given an offset. The magnitude of offset is 1.5% of peak-to-peak phase voltage amplitude. The results of this test are shown in Fig. 15. All the tested algorithms have undamped oscillation in frequency estimation, although magnitude of this oscillation is not large. Similar conclusion is drawn in [9].

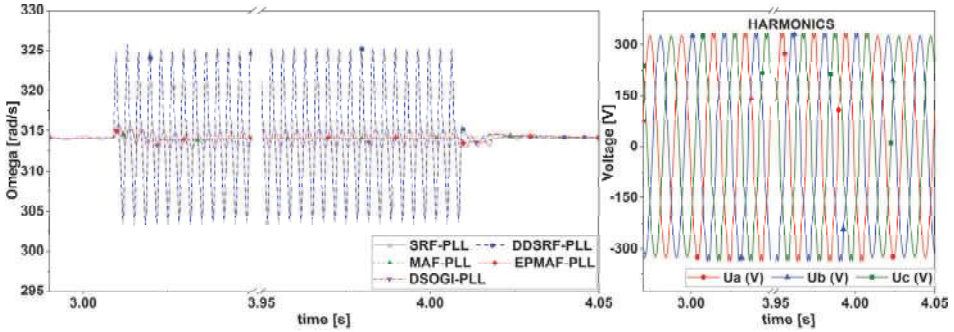

Fig. 14 – *Response of algorithms in the case of harmonics presence.*

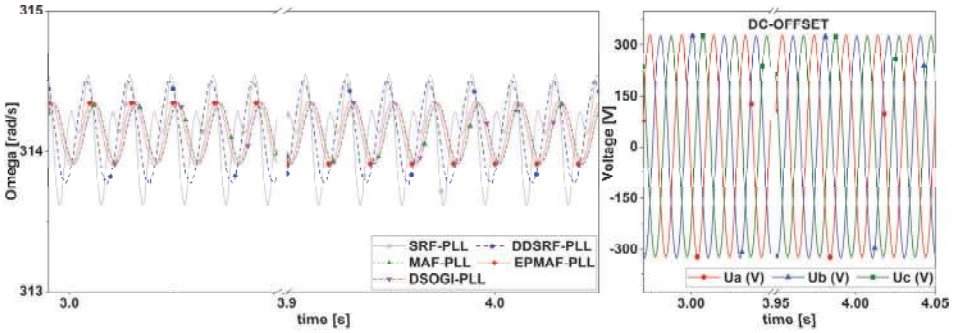

Fig. 15 – *Response of algorithms in the case of DC-offset presence.*

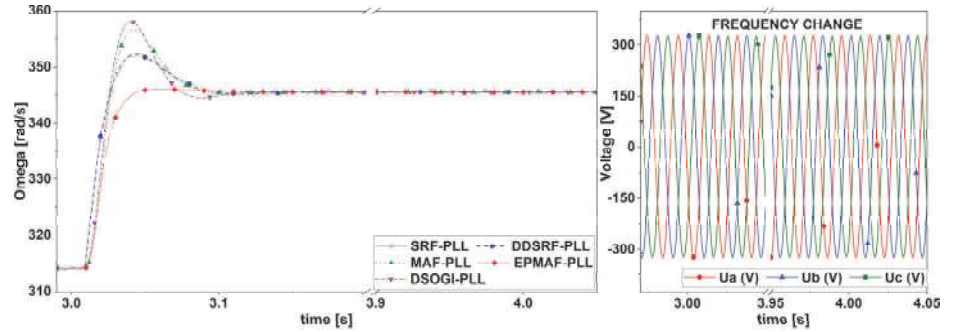

Fig. 16 – *Response of algorithms in the case of frequency change.*

Step change in the grid voltage frequency is the fourth test. The responses for all tested algorithms for a step change of frequency (from 50 Hz to 55 Hz) are shown in Fig. 16.

All algorithms showed frequency change tracking ability, with differences in transition period. All algorithms, except EPMAF-PLL type 2, had an overshoot and similar settling time. EPMAF-PLL type 2 showed best frequency change tracking ability. All algorithms in frequency step change test have

similar settling time to each other and some are substantially different than in [9], due to the fact that all controllers in these tests are tuned with the same natural frequency and damping ratio.

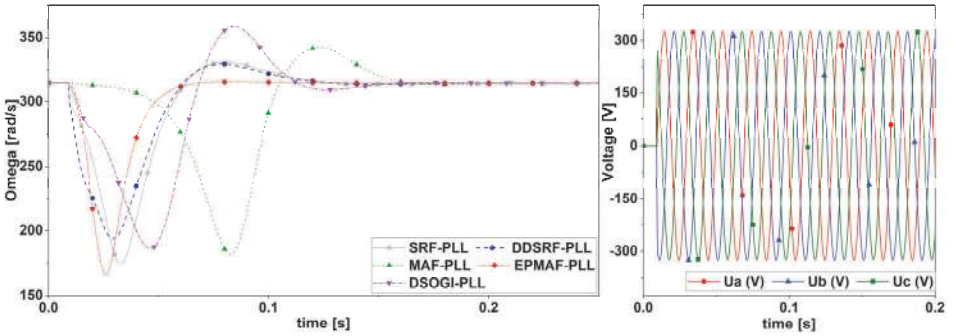

Fig. 17 – *Response of algorithms in the case of initial synchronization.*

Response of PLLs during initial grid synchronization is the last test. During synchronization period, grid voltages are kept nominal without any disturbances. Behaviour of the tested algorithms can be seen in Fig. 17.

Arguably, EPMAF-PLL type 2 had the fastest, while MAF-PLL had the slowest grid frequency lock in initial synchronization test.

5 Conclusion

Disturbances in grid voltage can affect ability of synchronization algorithm to precisely estimate phase angle. This paper shows detail comparison of popular three phase synchronization algorithms' frequency estimation in the events of sags, harmonics, DC offset, frequency change and initial synchronization.

Main findings of the paper are grouped in frame of tests:

Voltage sags: SRF-PLL showed no problem in grid voltage phase angle tracking during type A voltage sag. For all other unsymmetrical sags, it was the only tested algorithm with appearance of undamped oscillation. DDSRF-PLL algorithm provides excellent properties in grid voltage phase angle tracking during all sags. MAF and EPMAF type 2 PLL eliminated inverse sequence component successfully during all voltage sags. DSOGI-PLL had no problem in inverse voltage sequence elimination during voltage sags and therefore perfectly follows the network angle during these power quality events.

Voltage harmonics: SRF-PLL and DDSRF-PLL are not able to track only fundamental voltage harmonic during test with higher harmonics. MAF and EPMAF type 2 were able to lock on the fundamental frequency one window

length after harmonic occurrence (10 ms). DSOGI-PLL harmonics rejection capability is better than SRF and DDSRF-PLLs.

DC offset: all tested algorithms have a problem with undamped oscillations. In the case of MAF and EPMAF type 2 PLLs, these undamped oscillations could be rejected with the appropriate window length setup (20ms).

Frequency change and initial synchronization: All tested algorithms showed good frequency change tracking ability.

The main conclusion of this paper is that EPMAF-PLL type2 shows the best performance in the cases that have been tested and represents the most promising candidate for further practical applications.

6 Acknowledgments

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