SERBIAN JOURNAL OF ELECTRICAL ENGINEERING
Vol. 15, No. 3, October 2018, 285-300

UDC: 621.313.333:629.3 **DOI: https://doi.org/10.2298/SJEE1803285R**

Decoupled Centric and Non-Centric PWM Techniques for Open-End Winding Induction Motor Drive

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Abstract: This article proposes the space vector based decoupled centric and non-centric PWM techniques for open-end winding induction motor drive. To make the proposed configuration, 2-coventional inverters are fed on either side of open-circuited stator winding of induction motor. Therefore three level output is achieved. To obtain the control pulses for inverters in the proposed configuration reference sinusoids are used. All the proposed PWM techniques use the equal switching frequency. To obtain the validation for the proposed work various theoretical and simulation analysis is carried out using v/f control and the corresponding output voltage is verified experimentally using 1HP asynchronous motor.

Keywords: Centric PWM (CPWM), Decoupled, Non-centric PWM (NCPWM), Open-end winding Induction Motor (OEWIM).

1 Introduction

AC drives are generally employed in industries as high power drives. PWM voltage source inverters (VSI) are used to control the high power AC drives. Various PWM techniques are proposed in [1 − 7] namely, sine PWM (SPWM), Space vector PWM (SVPWM), Discontinuous PWM techniques. These PWM techniques are used to generate the control signals for the VSI. Therefore output voltage and frequency of VSI gets controlled. In conventional SVPWM technique, null vector shares the equal time along with the two active vectors with in a sampling period (T_s). This technique is also called centric PWM (CPWM) because of placing the active vectors at the middle of the sampling period. There are some discontinuous PWM (DPWM) techniques are also proposed in [1 – 7]. DPWM techniques are also called as non-centric PWM

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(NCPWM) techniques because of the placement of active vectors are not at the middle of the sampling period like CPWM. In DPWM techniques one of the phase is clamped to either positive link voltage or negative link voltage by 120^o of fundamental voltage cycle [1 – 7]. In DPWM techniques if any one phase is clamped to positive link voltage for 120^o then that PWM is positive bus clamping PWM. Similarly, if any one phase is clamped to negative link voltage for 120^o then that PWM is negative bus clamping PWM [3 – 7]. The main disadvantage of both positive and negative bus clamping PWM techniques is clamping of phases is done continuously for 120^o leads to more conduction loss [3 – 7]. To reduce this effect by splitting the clamping period instead of continuous 120^o. For obtaining this there are some advanced bus clamping PWM techniques like 60^o DPWM and 30^o DPWM are proposed [3 – 7]. In 60^o DPWM, clamping of phase is done within a half cycle of fundamental voltage. But in 30^o DPWM clamping of phase is done within a quarter cycle of fundamental voltage [3 – 7]. In general conventional inverters are suffered from a large common-mode voltage (CMV).This results the flow of bearing currents and electromagnetic interference. To eliminate the above mentioned drawbacks in conventional inverters a new configuration is proposed [8 – 12].

In this article, space vector based decoupled CPWM and NCPWM techniques are proposed for OEWIM drive. To obtain the control signals for the 2-conventional inverters used in the proposed configuration reference sinusoids are used. A CMV is reduced by great extent using proposed PWM techniques. All the proposed PWM techniques are implemented with constant switching frequency. To authenticate the proposed work several simulation studies have been carried out in v/f controlled induction motor drive and the corresponding output voltage is verified in real time.

2 Decoupled Open-End Winding Induction Motor Drive (DOEWIMD)

Fig. 1 shows the schematic of open-end winding Induction motor drive. Where V_{RX}, V_{YX} and V_{BX} denote the pole potentials of Inv-I and $V_{R'X'}$, $V_{Y'X'}$ and $V_{B'X'}$ denote the pole potentials of Inv-II. In this configuration, two conventional two level inverters are fed with separate dc supply to arrest the flow of zero sequence currents into the motor. The individual pole voltages of Inv-I and Inv-II are $V_{dc}/2$ or $-V_{dc}/2$ [8 – 11].

The effective phase voltage of this configuration is given by

$$V_{ZXZ'X'} = V_{ZX} - V_{Z'X'} \tag{1}$$

where $Z = R,\ Y,\ B$.

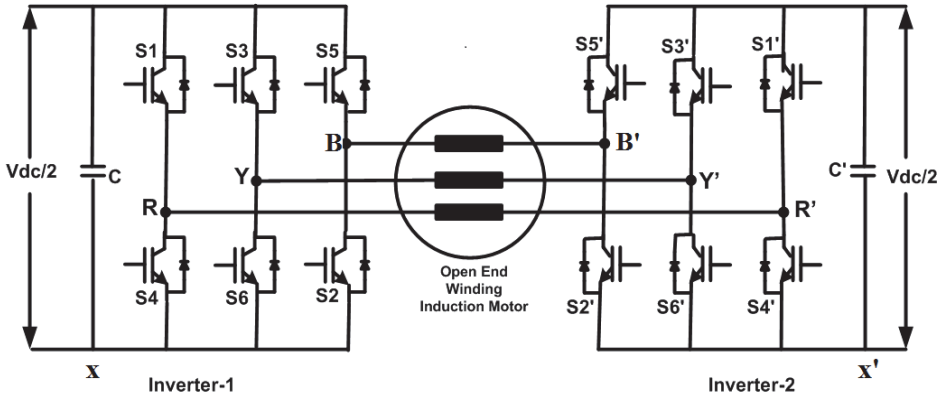


Fig. 1 – *Symmetrical dual inverter fed OEWIM drive [12].*

The CMV across the terminals X and X' is given by [8 – 11]

$$V_{XX'} = \frac{V_{RR'} + V_{YY'} + V_{BB'}}{3}. \tag{2}$$

3 Proposed PWM Techniques

All the proposed PWM techniques are implemented using space vector based decoupled approach. To generate the control pulses for Inv-I and Inv-II instantaneous phase sinusoids are used. Let VX1, VY1, VZ1 are the reference sinusoids of Inv-I and VX2, VY2, VZ2 are the reference sinusoids of Inv-II shown in equations (3) and (4) respectively. To generate the various PWM techniques proposed in this work are obtained by phase delaying the Inv-II reference voltages by 180^o with Inv-I voltages as reference [12].

$$\begin{aligned} VX1 &= V_m \cos\omega t \\ VY1 &= V_m \cos(\omega t - 120^0) \\ VZ1 &= V_m \cos(\omega t - 240^0) \end{aligned} \tag{3}$$

$$\begin{aligned} VX2 &= V_m \cos(\omega t - 180^0) \\ VY2 &= V_m \cos(\omega t - 120^0 - 180^0) \\ VZ2 &= V_m \cos(\omega t - 240^0 - 180^0) \end{aligned} \tag{4}$$

3.1 Centric PWM (CPWM)

In CPWM technique zero vector is used twice in a half carrier cycle [3 – 7]. To generate switching sequence, Inv-1 is operated in sector-1(0^o), whereas Inv-2 is operated by 180^o advance with Inv-1 as reference is shown in Fig. 2.

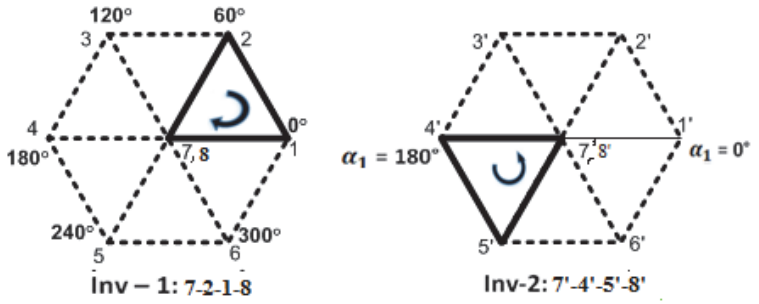


Fig. 2 – *Switching sequences of the individual inverters using CPWM technique.*

In CPWM, each phase is switches once in a sub-cycle and two sub cycles constitute a switching cycle.

3.2 Non-Centric PWM (NCPWM)

In decoupled NCPWM techniques (812/721) only one null state is used in a half switching cycle [3 − 7]. In NCPWM techniques, one of the phases is clamped to either positive or negative link voltage by 120°. Fig. 3 and Fig. 4 shows the switching sequences of NCPWM techniques. In NCPWM techniques Inv-I switches in sector-I, whereas Inv-II switches 180° advance with respect to Inv-I. In NCPWM1, B-phase is clamped to negative link voltage and the remaining phases are switches once in a sub-carrier cycle [5 − 7]. Whereas in NCPWM2 B-phase is clamped to positive link voltage and the remaining phases are switches once in a sub-carrier cycle [5]. Hence, the number of switchings in a sub-carrier cycle are reduced by 1/3rd of CPWM technique. Therefore switching loss becomes less in NCPWM techniques over CPWM technique.

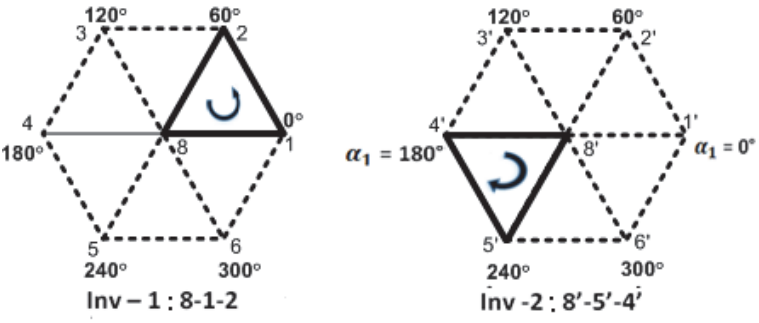


Fig. 3 – *Switching sequences of the individual inverters using NCPWM1.*

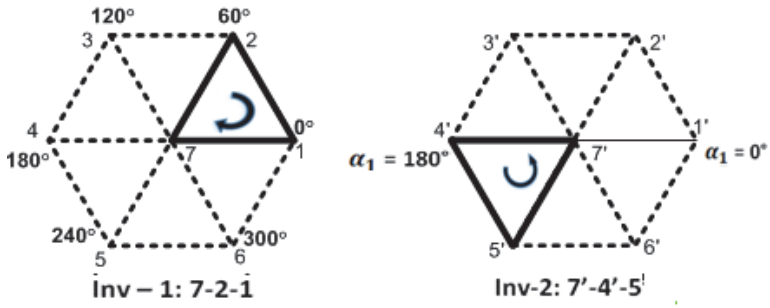


Fig. 4 – *Switching sequences of the individual inverters using NCPWM2.*

Though NCPWM techniques produce less switching loss over CPWM technique, there is an unbalance in loading of switches due to continual clamping of phases about 120°. To avoid this advanced non-centric PWM techniques are proposed in this work to reduce the unbalance loading of switches, hence the quality of output voltage is improved. Fig. 5 and Fig. 6 shows the switching sequences of advanced NCPWM1 and advanced NCPWM2 techniques.

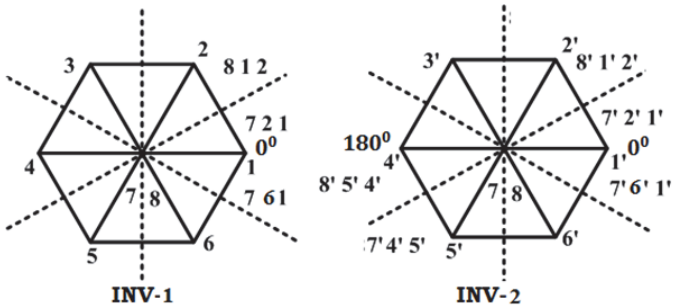


Fig. 5 – *Switching sequences of the individual inverters using advanced NCPWM1.*

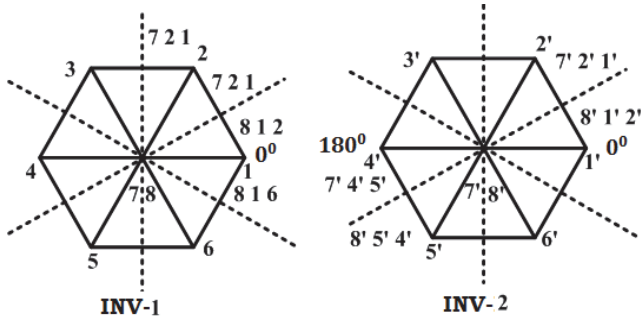


Fig. 6 – *Switching sequences of the individual inverters using advanced NCPWM2.*

In advanced NCPWM1 method within each sector both the non-centric PWM sequences are used. It results the clamping of phases takes place of 60^o. This PWM technique is also known as 60^o NCPWM technique. Similarly in advanced NCPWM2 method within each sector alternate non-centric PWM sequences are used than 60^o NCPWM. It results the clamping of phases takes place of 30^o. This PWM technique is also known as 30^o NCPWM technique.

4 Results and Discussion

To authenticate the proposed work several simulation studies have been carried on v/f controlled OEWIM drive. Switching frequency is chosen for the simulation as well as for experimental study is 1000 Hz. Control signals for two inverters used in real time is obtained using Dspace board. A Digital Storage Oscilloscope (500V−3.3V) regulator is used to measure the output voltage. The motor parameters are considered for simulation are $R_s = 1.57\Omega$, $R_r = 1.21\Omega$, $L_m = 1.165\,\mathrm{H}$, $L_s = 1.17\,\mathrm{H}$, $L_r = 1.17\,\mathrm{H}$ and $J = 0.089\,\mathrm{kgm}^2$. Modulation Index for result analysis is chosen as 0.86.

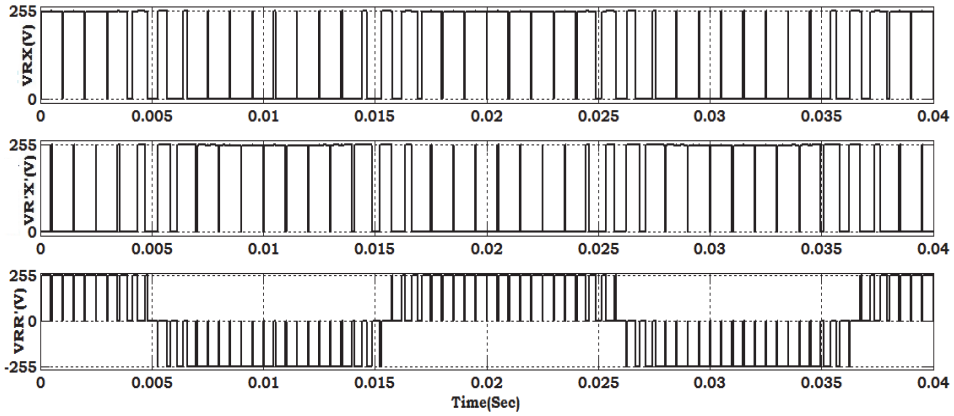
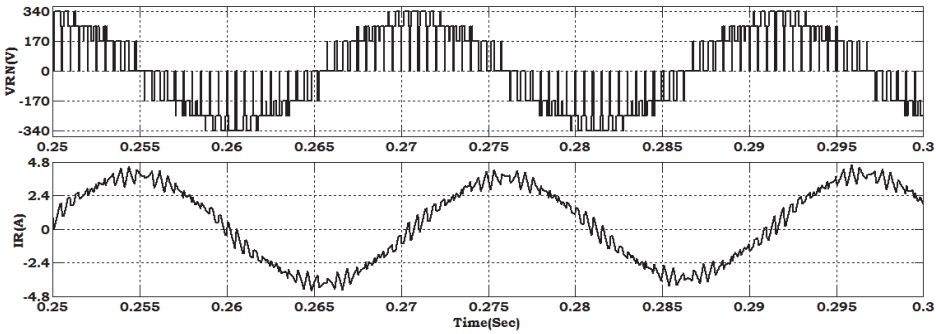
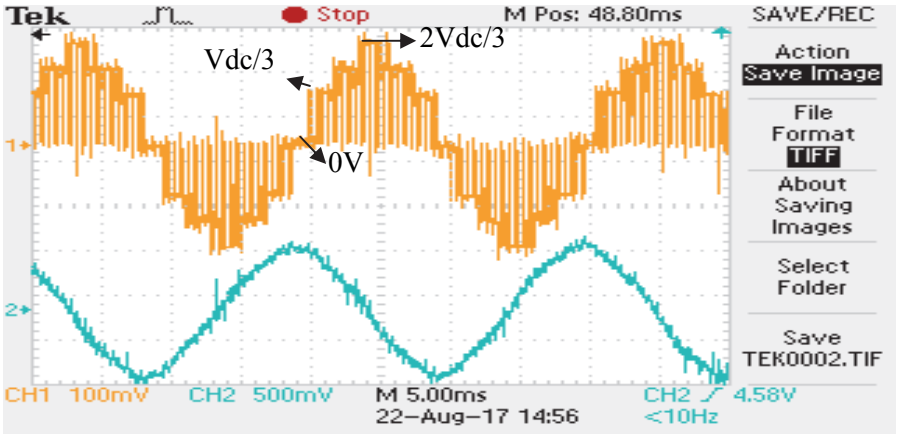


Fig. 7 – *Pole voltages of Inv-I and Inv-II and effective pole voltage (VRR') using CPWM.*

Fig. 7 shows the pole potentials of Inv-I and Inv-II along with the effective pole voltage of magnitude ± $V_{dc}/2$ (± 255V) respectively. From the pole potentials it is observed that continues switching of inverters takes place in a fundamental voltage cycle using CPWM technique. Figs. 8a and 8b shows the output phase voltage of the proposed configuration both from simulation and real time using CPWM technique. From the output voltage traces it is identified that the 3-level output voltage of magnitude ± $2V_{dc}/3$(±340V) is achieved from the proposed configuration and the corresponding generated CMV of magnitude ±$V_{dc}/6$ (± 85V) from simulation as well as from real time are shown in Figs. 9a and 9b.

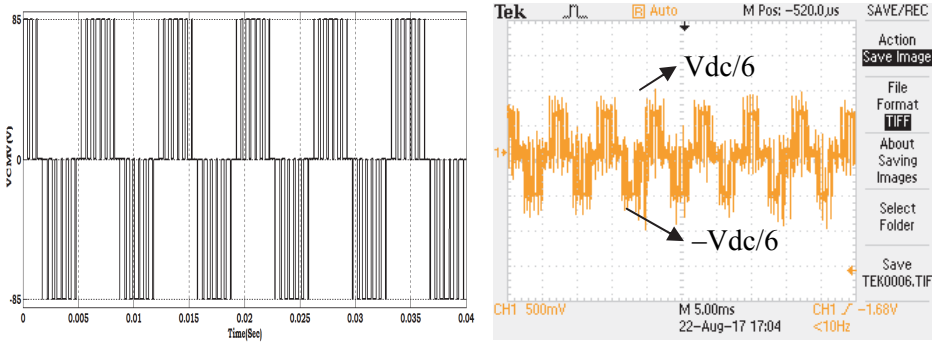


(a)



(b)

Fig. 8 – *Effective voltage and Line Current (IR) traces with CPWM from: a) Simulation; b) Real time.*



(a) (b)

Fig. 9 – *CMV profiles with CPWM from: a) Simulation; b) Real time.*

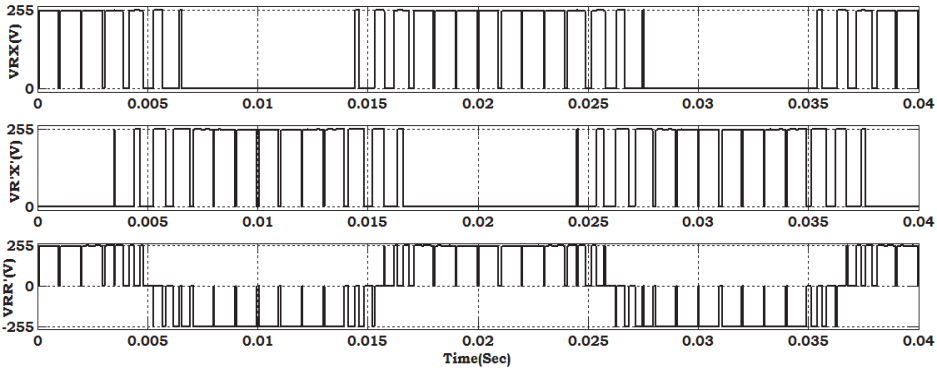
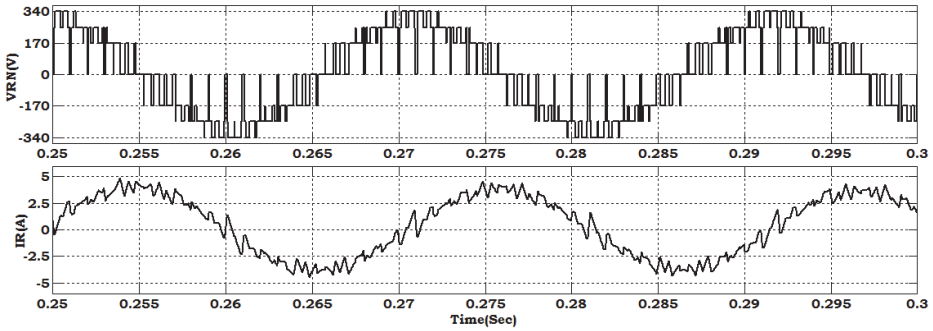
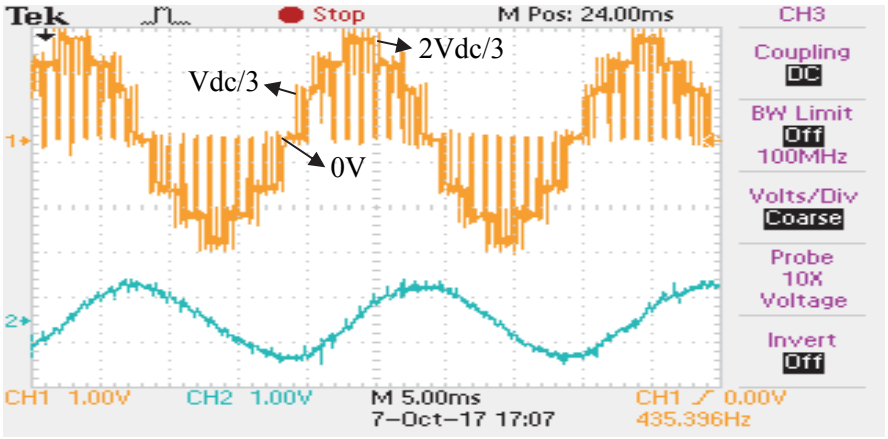


Fig. 10 – *Pole voltages of Inv-I and Inv-II and effective pole voltage (VRR') using NCPWM1.*

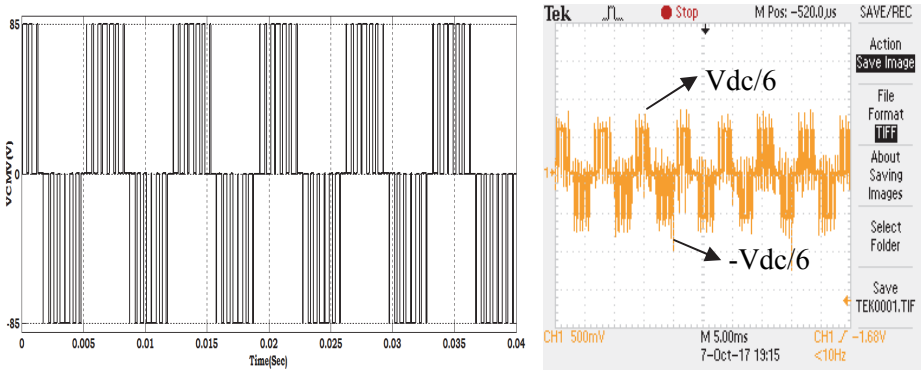


(a)



(b)

Fig. 11 – *Effective voltage and Line Current (IR) traces with NCPWM1 from: a) Simulation; b) Real time.*



(a) (b)

Fig. 12 – *CMV profiles with NCPWM1 from: a) Simulation; b) Real time.*

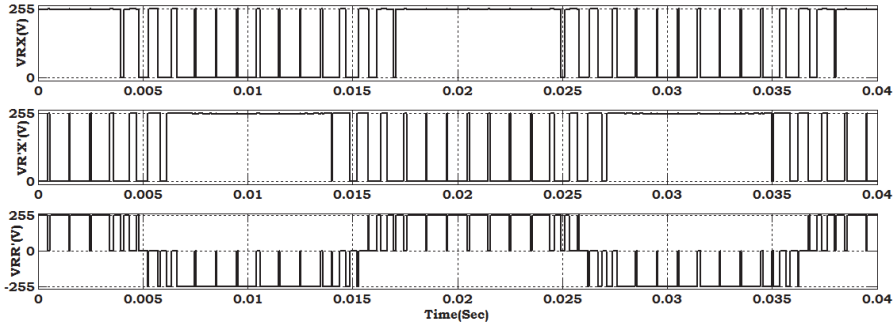
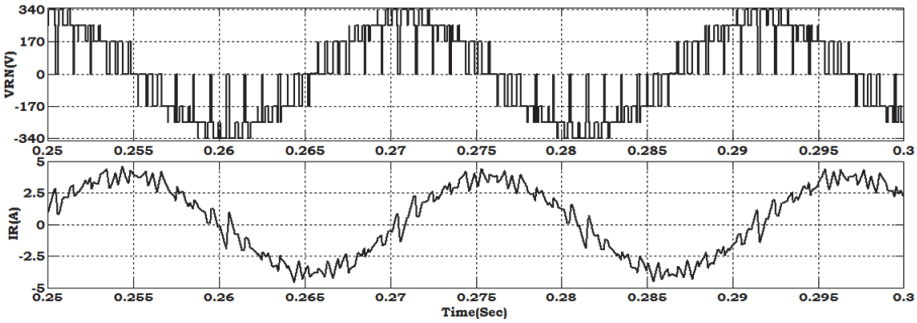
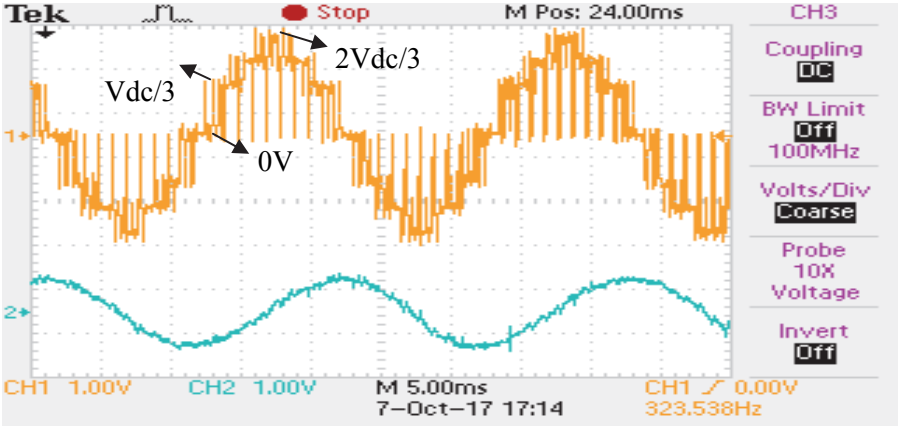


Fig. 13 – *Pole voltages of Inv-I and Inv-II and effective pole voltage (VRR') using NCPWM2.*

Figs. 10 and 13 show the pole potentials of Inv-I and Inv-II along with the effective pole voltage of magnitude $\pm V_{dc}/2$ (±255V) using NCPWM1 and NCPWM2 techniques. From the pole voltages it is identified that there is a clamping of phases by 120° of fundamental voltage cycle. This result the number of switchings per cycle got reduced by and hence the switching loss becomes 33% over CPWM technique both in NCPWM1 and NCPWM2 techniques. Figs.11 and 14 shows the corresponding output phase voltages of magnitude $\pm 2V_{dc}/3$ (±340V). A CMV of magnitude $\pm V_{dc}/6$ (±85V) is also observed from both NCPWM1 and NCPWM2 techniques. Fig. 16 gives the information of the pole potentials of the inverters used in the proposed configuration along with the effective pole voltage using advanced NCPWM1 technique. Hence it is observed that the clamping of phases takes place by 60° in advanced NCPWM1 technique within the half cycle of the fundamental cycle. Similarly, Fig. 19 shows the pole potentials of the inverters using advanced NCPWM2 technique. It is observed that the clamping of phases takes place by 30° in advanced NCPWM2 technique within the quarter cycle of the fundamental voltage.

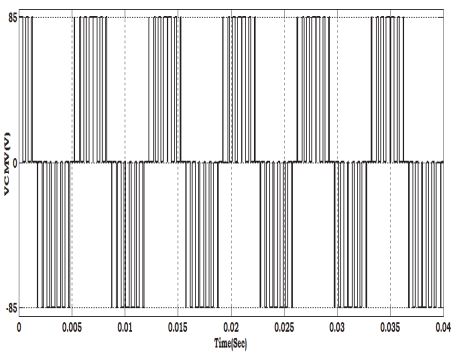


(a)

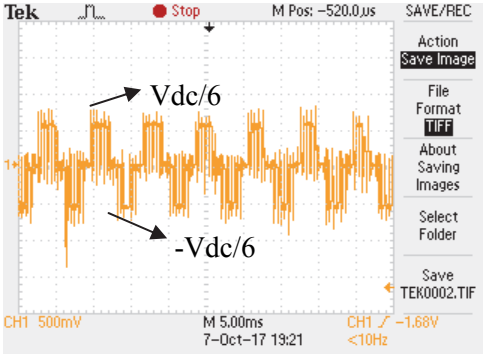


(b)

Fig. 14 – *Effective voltage and Line Current (IR) traces with NCPWM2 from: a) Simulation; b) Real time.*



(a)



(b)

Fig. 15 – *CMV profiles with NCPWM2 from: a) Simulation; b) Real time.*

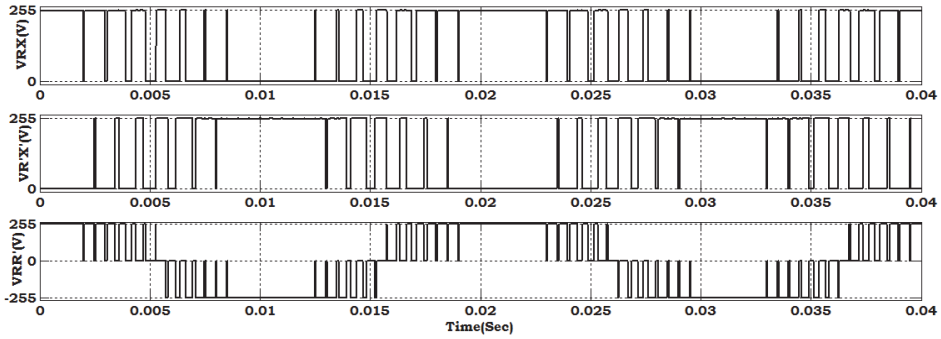
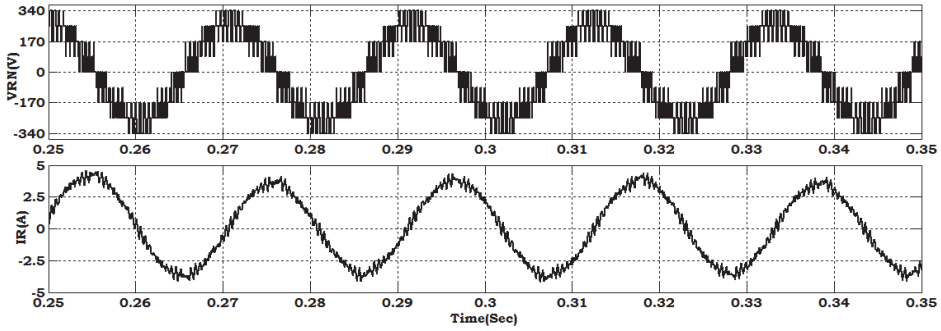
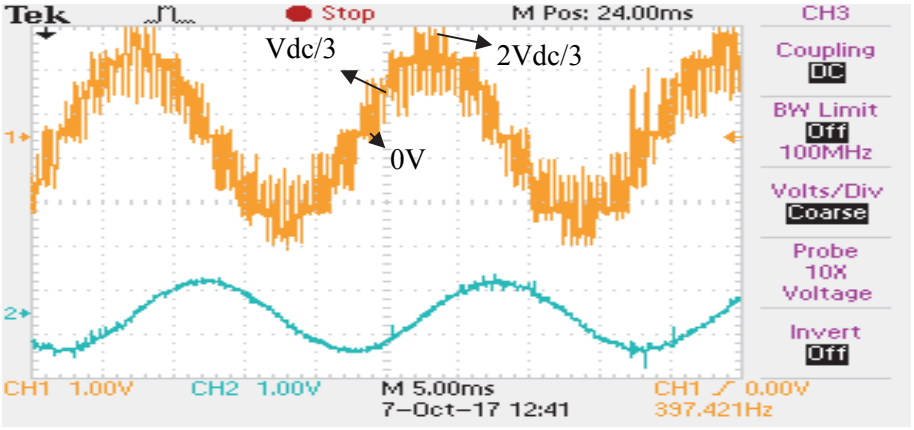


Fig. 16 – *Pole voltages of Inv-I and Inv-II and effective pole voltage (VRR') using advanced NCPWM1.*



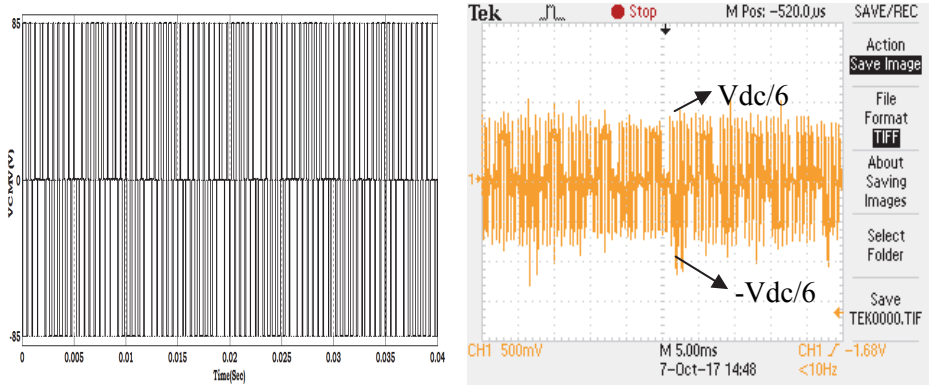
(a)



(b)

Fig. 17– *Effective voltage and Line Current (IR) traces with advanced NCPWM1 from: a) Simulation; b) Real time.*

From Figs. 17 and 20 it is found that the quality of output voltage is improved in advanced NCPWM methods than the other methods proposed in this work. But the magnitude of CMV increases shown in Fig. 21 to $\pm V_{dc}/3$ (±170V) in advanced NCPWM2 method over the other methods proposed in this work. Fig.18 shows the CMV of the proposed configuration using advanced NCPWM1 method. Harmonic samples of the proposed methods are shown in Fig. 22. From Fig. 22a, it is observed that the in CPWM technique more number of samples are concentrated at first side band (2fc) of switching frequency (around 2000 Hz). Similarly, Figs. 22b and 22c shows the harmonic samples of NCPWM1 and NCPWM2 techniques. It is observed that in NCPWM techniques, concentration of more harmonic samples at both at 1000 Hz and 2000 Hz. This is due to the reduction in switching frequency in NCPWM techniques by 66% over CPWM technique.



(a) (b)

Fig. 18 – *CMV profiles with advanced NCPWM1 from: a) Simulation; b) Real time.*

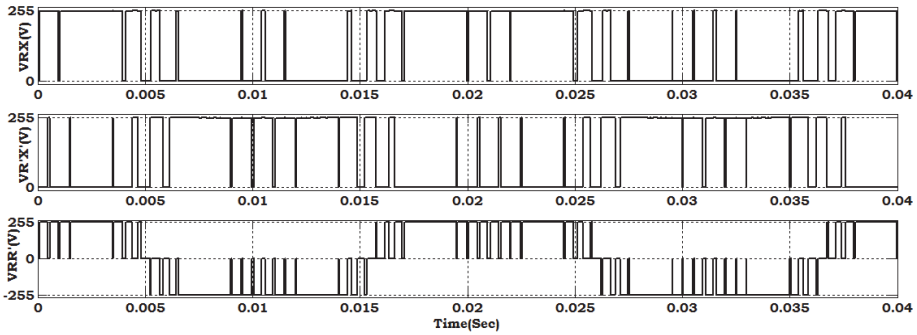
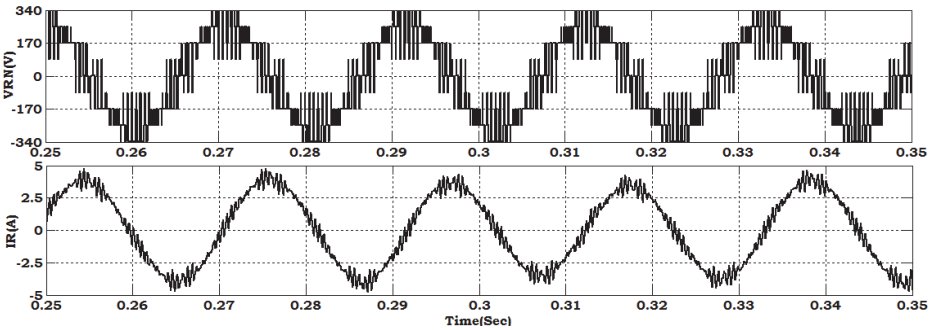
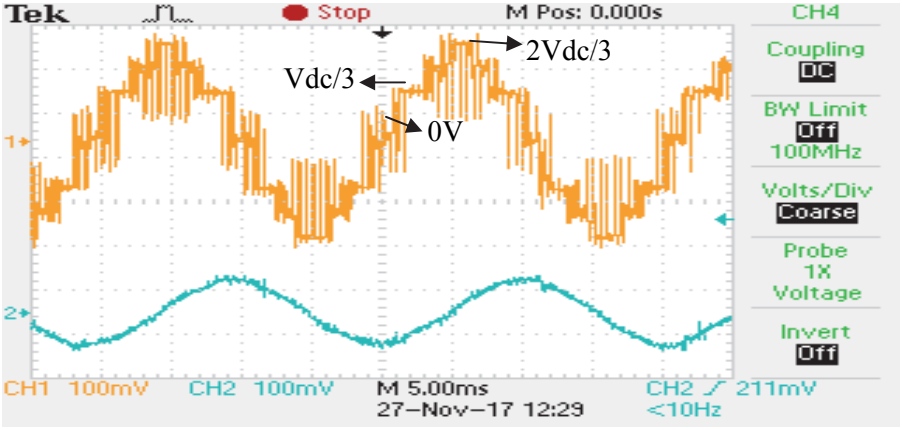


Fig. 19 – *Pole voltages of Inv-I and Inv-II and effective pole voltage (VRR') using advanced NCPWM2.*

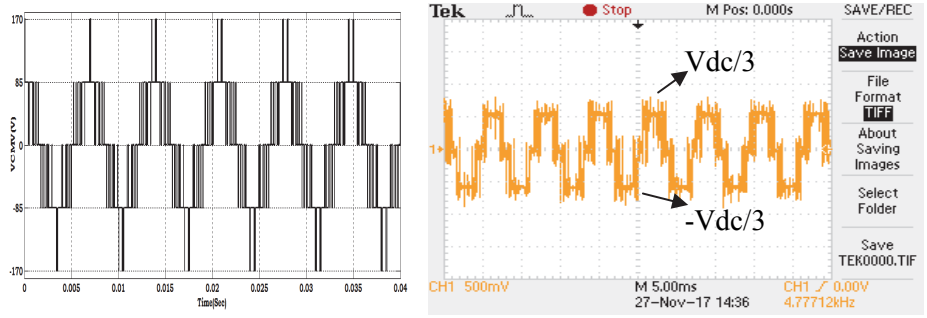


(a)



(b)

Fig. 20 – *Effective voltage and Line Current (IR) traces with advanced NCPWM2 from: a) Simulation; b) Real time.*



(a) (b)

Fig. 21 – *CMV profiles with advanced NCPWM2 from: a) Simulation b) Real time.*

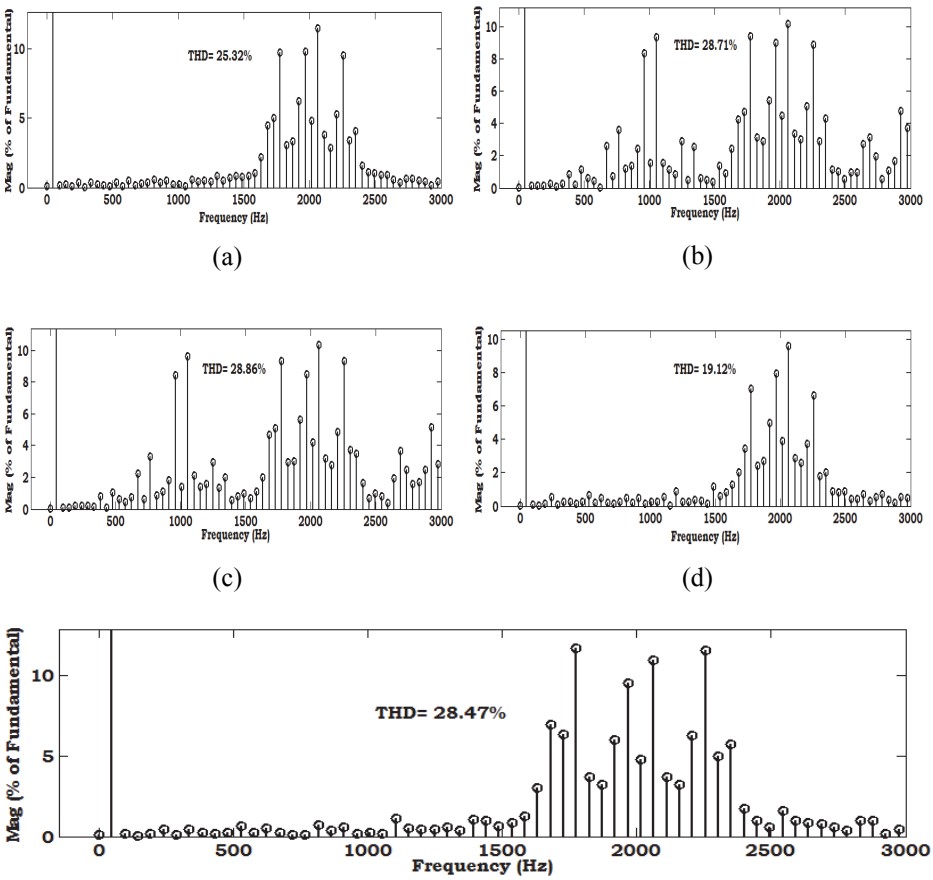


Fig. 22 – *Harmonic samples of phase voltage (VRN) using: a) CPWM; b) NCPWM1; c) NCPWM2; d) Advanced NCPWM1; e) Advanced NCPWM2.*

This result the frequency got reduced at 1000 Hz and 2000 Hz makes the less reactance offered by the machine results the more conduction in the band of frequencies (1000 Hz and 2000 Hz). Figs. 22d and 22e shows the harmonic samples of advanced NCPWM techniques. Hence it is observed that advanced NCPWM1 method is superior to other methods in generation of harmonics in output voltage.

5 Conclusion

In this article, space vector based decoupled CPWM and NCPWM techniques are proposed for OEWIM drive. To obtain the control signals for the

2-conventional inverters used in the proposed configuration reference sinusoids are used. To validate the various simulations performed on v/f control of OEWIM drive 1Hp motor is used to authenticate the same in real time. From the result analysis it is concluded that the CPWM technique is superior at generation of reduced CMV of magnitude $\pm V_{dc}/6$ (±85V), but it is inferior to quality of output phase voltage. Similarly NCPWM techniques reduce the switching loss by 33% over CPWM; however conduction loss becomes severe due to unequal loading of top and bottom switches of the inverters. In advanced NCPWM2 technique quality of output voltage is improved by increasing the step size to achieve the three level output. But it is inferior over the other methods in CMV point of view. Therefore, advanced NCPWM1 method is superior to all proposed methods in both output voltage quality and reduced CMV generation.

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