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A High Efficiency Non-Inverting Multi Device Buck-Boost DC-DC Converter with Reduced Ripple Current and Wide Bandwidth for Fuel Cell Low Voltage Applications

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Abstract: The voltage produced by the fuel cell (FC) device is unregulated and varies from 0.4 V to 0.8 V on full load to no-load respectively. When these devices are used in low voltage applications and output voltage lies between higher and lower values of input voltage range, it is required to connect a DC-DC buck-boost converter to get a fixed output voltage. In this paper, a new non-inverting multi device buck boost converter (MDBBC) is proposed, in which the multi device buck and boost converters are connected in cascade and operate individually either in buck or boost operating modes. The paper also includes the steady state analysis of MDDBC based on the state space averaging technique. A prototype model of proposed converter compatible with FCS-1000 Horizon FC model with rating of 270 W, 36 V is designed and developed. The proposed converter is experimentally validated with the results obtained from the prototype model, and results show the superiority of the converter with higher efficiency and lesser ripple current observed under steady state operation of the converter.

Keywords: Buck-Boost Converter, Multi Device Operation, Ripple Current Reduction, Buck-Boost Converters for Portable Applications.

1 Introduction

Fuel cell (FC) is a device which produces electrical energy by using the chemical energy of a fuel. The individual voltage of a single cell ranges from 0.4 V to 0.8 V from full load to no load respectively which gives a voltage regulation of approximately 100% [1]. As an individual cell voltage is very less, several FCs may be connected in series to form a stack and can realize the voltage requirement of the practical systems. For example, the *Horizon FC model "FCS-1000"* with 48 cells gives a rated voltage of 28 V at loaded condition and 45 V at no load. In many low power/voltage applications like battery charging/discharging, power factor correction and for extracting

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maximum power from solar photovoltaic (PV) panels, buck- boost converters may be used in obtaining a regulated voltage. As the fuel cell voltage is unregulated, step up/step down converter is compulsory to obtain a regulated output voltage which lies within the terminal voltage range of the FC stack [2 – 14]. The commonly used simple step up/step down converters buck-boost, Sepic, Cuk, and fly back topologies when used in the aforementioned applications, exhibits low efficiency, high device stress, and requires large value of filter inductor and capacitors and higher conduction losses [2].

In order to avoid high device stresses, paralleling or interleaved coupled inductors [3] and multilevel techniques are suggested in [4, 5]. But neither of the above approaches reduced voltage stress and current stress simultaneously. In order to achieve low device stress, high efficiency, lesser size of filter components, a cascaded buck-boost converter with independent controlled switches is suggested in [6], in which the converter operates only either in boost mode or buck mode depends on the input-output conditions. In [7 – 11] a non-inverting buck–boost converter (combining the boost and buck together results in single inductor) with high performance suitable for low voltage applications is suggested. But for higher voltages the usage of single inductor non–inverting buck boost converters results in high I/O pulsating currents, high noise levels, difficulty to control and limit the currents, to eliminate these problems a double inductor (one at the input and other at output) cascaded buck-boost converter has been proposed by [12 – 14].

A single phase cascaded buck-boost converter (BBC) with magnetic coupling between input inductor and output filter inductor has been proposed in [15], which reports higher efficiency, wide bandwidth, reduced input and output capacitor sizes, but the ripple current remains high. To overcome which a tri-state two switch buck- boost converter is have been proposed in [16], but the larger boost inductor is preferred which increases the size. Furthermore, some researchers have suggested pseudo CCM method to reduce the FC ripple current further [17, 18]. A two phase interleaved buck-boost converter (IBBC) with fewer ripples in the input current has been proposed in [19, 20]. Apart from the above mentioned BBC and IBBC another possible method is multi device technique, in which the component size of inductive and capacitive filters on input and output are reduced by simply increasing the frequency of ripple current in the inductor using parallel switches in a phase [21], however the switching and conduction losses, device stress, and number of current sensors are same as that of device switch buck-boost converters.

This paper presents a new multi device buck–boost converter (MDBBC) for FC low power applications. In MDBBC two switches are connected in parallel on buck and boost side as illustrated in Fig. 1a, resulting in a single inductor, doubling in effective switching frequency of the inductor ripple

current and thereby reducing the sizes of I/O filter components with higher bandwidth and same fault tolerance capability as IBBC. Further, the steady state operation of the proposed converter and state equations are derived on considering certain operating conditions and there by the circuit design and implementation suitable for FC voltage regulation is presented. A prototype model of proposed converter is developed with 270 W, 36 V rating, which suits for FC voltage regulation purpose.

2 Proposed MDBBC Structure

The structure of MDBBC is depicted in Fig. 1a and consists of two switches and diodes connected in parallel per phase. By using multi devices per phase the sizes of the filter components are reduced by increasing the effective inductor ripple frequency and voltage ripple frequency. A phase shifting mechanism is used to provide the doubled ripple frequency (100 kHz) in the buck and boost inductors ripple current at the same device switching frequency (50 kHz), which can provide a larger system bandwidth. The larger bandwidth helps in achieving the high speed dynamic response for the converter and also reduces the sizes of the filtering components.

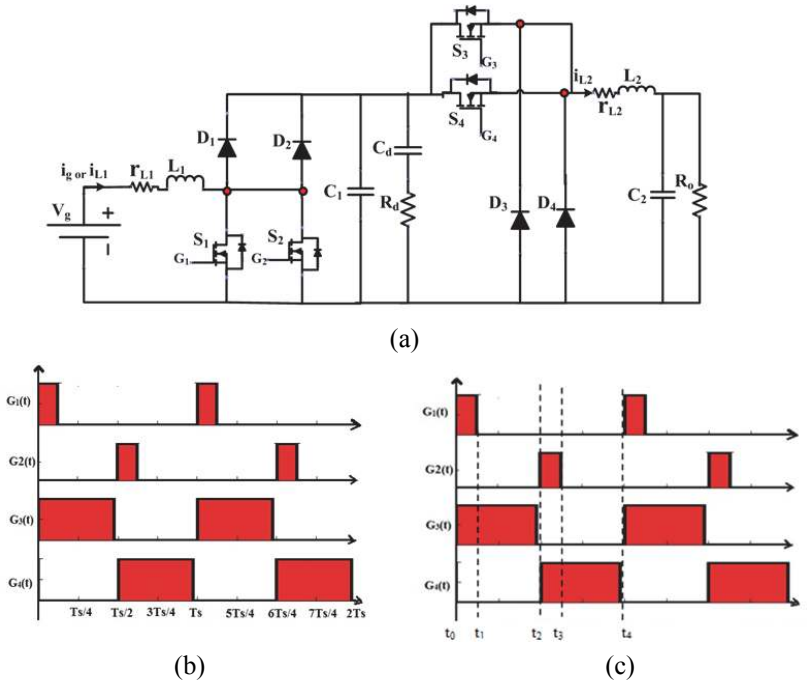


Fig. 1 – *Proposed converter and operating modes: a) schematic circuit of the proposed converter; b) Activation signals for the buck and boost switches; c) operating modes of the converter in both buck and boost operations.*

Further, in order to provide the doubled ripple frequency in the inductor ripple current, the selected sequence of driving signals for the MDBBC switches are shown in Fig. 1b. In the proposed MDBBC the switching pattern for the switches is shifted by 360º/($p \times q$), where 'p' is no. of phases in the converter and 'q' is no. of parallel switches and diodes per phase [31]. The input ripple current frequency is ($p \times q$) times the switching frequency. Similarly, the switching frequency of the voltage ripples in filter capacitors is ($p \times q$) times the switching frequency, which results in reduction of filter component sizes by *'q'* times as that of conventional single switch buck-boost converter. In this proposed converter *'p'* is chosen to be 1 and while 'q' is selected to be 2. Fig. 1c demonstrates the switching pattern sequence of the activation signals for the four operating modes. Further, the equivalent circuit diagrams under the four operating intervals based on the chosen switching pattern are illustrated in Fig. 2. Here, continuous conduction mode is assumed for the analysis of steady state behaviour of the converter. The switches S_1 and S_2 have identical duty cycles, i.e., $d_1 = d_2 = d_{12} = 0.1$ and S_3 and S_4 have the duty cycles of $d_3 = d_4 = d_{34} = 0.5$, where'd' is the duty cycle.

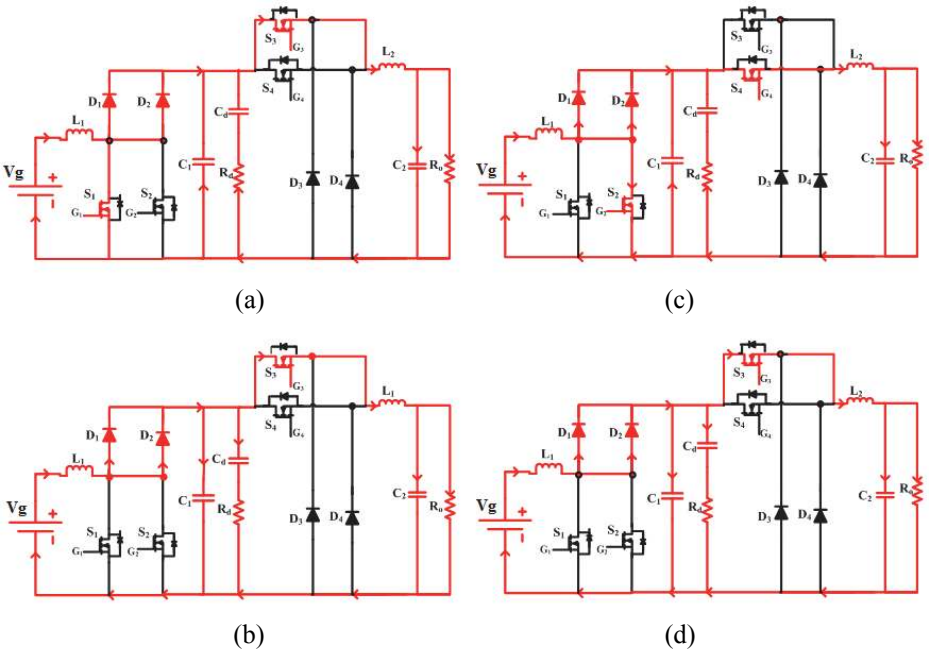


Fig. 2 – *Conduction diagrams of MDBBC for duty cycle* $d_1 = d_2 = d_{12} = 0.1$ *and* $d_3 = d_4 = d_{34} = 0.5$*: a) Conduction diagram for Mode I:* $t_o \le t \le t_1$*; b) Conduction diagram for Mode II:* $t_1 \le t \le t_2$*; c) Conduction diagram for Mode III:* $t_2 \le t \le t_3$*; d) Conduction diagram for Mode IV:* $t_3 \le t \le t_4$.

3 Principle of Operation and Steady State Behaviour of the Proposed Converter

The proposed MDBBC converter is operated in both buck and boost modes of operation as shown in Figs. 3a and 3c, respectively. In boost operating mode the switches S_1 and S_2 are operated in PWM and S_3 and S_4 are continuously on in a half cycle with 50% duty cycle, similarly in the buck mode of operation switches S_3 and S_4 are operated in PWM while S_1 and S_2 remains off. The waveforms in Figs. 3b and 3d portray the steady state characteristics of MDBBC in both buck and boost operating modes respectively.

The duty cycles for the switches S_1 and S_2 are considered as $d_{12}(t)$ and for S_3 and S_4 it is $d_{34}(t)$. The duty cycles of the switches are adjusted to get the output voltage of around 36 V in both buck and boost modes of operation. In fuel cell applications it is necessary that the input ripple current must be lower than 5% of normal rated value to ensure the satisfactory FC operation [22, 23].One can scrutinize the ripple percent in Figs. 3b and 3d as only less than 4% with the proposed converter.

Also the capacitor voltage ripple is less and lies between 0.2 and 0.4 V. The presence of oscillations in the output voltage at the boundary of operation is attenuated by placing a damping network at the middle of boost and buck circuits [15]. The benefit of using damping network in reducing output voltage oscillation is explained in [24] using the frequency and time domain analysis.

Moreover, employing the multi device technique in addition to the interleaving can further reduce the input current and voltage ripples, reduce converter size and increase efficiency and such buck-boost converters are best suitable for medium power applications. For elaborating the fundamental principles of operation and obtaining the state equations of the proposed converter in buck and boost operating modes the selected switching pattern is shown in the Fig. 3c.

The switching strategy chosen ensures all the possible switching states in a time period. In Mode I, S_1 and S_3 are conducting while S_2 and S_4 are switched off, in Mode II, S_3 is on and the remaining switches S_1, S_2 and S_4 are turned off, in Mode III, the switches S_2 and S_4 are conducting while S_1 and S_3 are turned off, in Mode IV, the switch S_4 is only turned on and remaining S_1, S_2 and S_3 are switched off.

The differential equations of the converter in both operating modes can be written by assuming the continuous conduction mode. In one time period there are four operating intervals available and further the corresponding equivalent circuit diagrams representing the voltage drops and current distribution at nodes are illustrated in Fig 4. Further, in order to obtain the differential equations the popular method called state space averaging method [2] is used. Similarly the other method called signal flow graph [25] can also be used for deriving the transfer functions to evaluate the dynamic performance of the converter.

The operating modes of the converter can be explained in four operating modes as follows:

Mode I: $t_o \le t \le t_1$**:** At time t_o the switches S_1 and S_3 are turned on, then the inductor L_1 starts storing energy in it. The stored energy in the inductor L_1 transfers to the load (as the switch S_3 is conducting, the input energy can reach output side through the path formed). The conduction path is demonstrated in the Fig. 2a. Further, the corresponding equivalent circuit is shown in the Fig. 4a and the inductor currents and capacitor voltage equations are shown in (1).

Mode II: $t_1 \le t \le t_2$**:** At time t_1 only S_3 is conducting while S_1, S_2 and S_4 are turned off, the energy emanated from the source reaches load through the conducting switch S_3 the energy transfers from source to load through the conduction path shown in Fig. 2b. The corresponding equivalent circuit is depicted in Fig. 4b. Here the capacitor C_1 supplies the demanded load current, whereas C_d charges. The set of differential equations for this mode similarly can be written as done in mode I. the related equations are presented in *Appendix-1*(A_1).

$$
\begin{aligned}
v_{L1}(t) &= L_1 \frac{\mathrm{d}\, i_{L1}(t)}{\mathrm{d}\, t} = v_s(t) - v_{c1}(t), \\
v_{L2}(t) &= L_2 \frac{\mathrm{d}\, i_{L2}(t)}{\mathrm{d}\, t} = v_{cd}(t) - v_o(t) \quad \text{or} \quad v_{c1}(t) - v_o(t), \\
i_{c1}(t) &= C_1 \frac{\mathrm{d}\, v_{c2}(t)}{\mathrm{d}\, t} = i_{L1}(t) - (i_{cd}(t) + i_{L2}(t), \\
i_{cd}(t) &= C_d \frac{\mathrm{d}\, v_{cd}(t)}{\mathrm{d}\, t} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d} = i_x(t) - i_{L2}(t), \\
i_x &= i_c(t) + i_{L2}(t) \quad \text{or} \quad i_{L1}(t) - i_{c1}(t), \\
i_{c2}(t) &= C_2 \frac{\mathrm{d}\, v_{C2}(t)}{\mathrm{d}\, t} = i_{L2}(t) - \frac{v_o(t)}{R_o}.
\end{aligned}
\tag{1}
$$

Mode III: $t_2 \le t \le t_3$**:** At time t_2 the switches S_2 and S_4 are conducting while the other switches S_1 and S_3 are turned off, the energy emanated from the source appears at the load through the path as shown in Fig. 2c. The corresponding equivalent circuit is shown in Fig. 4c. The set of differential equations of voltage and current through the components are presented in *Appendix* (A_2).

Mode IV: $t_3 \le t \le t_4$**:** At time t_3 only the switch S_4 is conducting while the other switches S_1, S_2 and S_3 are turned off, the energy transfers from source to load through the conduction path as shown in Fig. 2d. The corresponding equivalent circuit representing voltages and currents is shown in Fig. 4d. In this mode also the C_1 discharges to aid the supply current, the set of differential equations for this mode similarly can be written. It is presented in *Appendix.* (A_3).

After analysing the individual modes of operation with clear differential equations, by applying SSA method to the converter model over a switching period, one can write the modelling equations as shown in (2) While applying this technique it is assumed that the circuit is operating in continuous conduction mode, parasitic effects are neglected, and the switching frequency is much higher than the converter's usual frequencies. On applying the technique following differential equations are obtained.

$$\begin{aligned}
L_1 \frac{\mathrm{d}\,\bar{i}\,L_1(t)}{\mathrm{d}t} &= v_s(t) - \bar{v}_{c1}(t)(1-d_{12}(t)),\\
L_2 \frac{d\bar{i}\,L_2(t)}{\mathrm{d}t} &= \bar{v}_{c1}(t)\big(1-d_{12}(t)\big) - \bar{v}_o(t),\\
C_1 \frac{\mathrm{d}\,\bar{v}_{c1}(t)}{\mathrm{d}t} &= \bar{i}\,L_1(t)\big(1-d_{12}(t)\big) - \bar{i}\,L_2(t)\big(1-d_{34}(t)\big) - \frac{\bar{v}_{c1}(t)-\bar{v}_{cd}(t)}{R_d},\\
C_d \frac{\mathrm{d}\,\bar{v}_d(t)}{\mathrm{d}t} &= -\frac{\bar{v}_{cd}(t)+\bar{v}_{c1}(t)}{R_d},\\
C_2 \frac{\mathrm{d}\,\bar{v}_o(t)}{\mathrm{d}t} &= \bar{i}\,L_2(t) - \frac{\bar{v}_o(t)}{R_o}.
\end{aligned} \tag{2}$$

The accent over a signal stands for averaging done in a switching period. d_{12} and d_{34} denotes that the duty cycles of the switches S_1, S_2 and S_3, S_4 respectively. The circuit based analysis for obtaining (2) is carried out when we replace with the time averaged models [26], which results in a large signal model as shown in Fig. 5a assuming the converter operating under steady state condition and the corresponding constant duty cycles are D_{12} and D_{34} and the input voltage $v_s(t) = V_s$, one can write expressions of capacitor voltages and inductor currents by applying the inductor volte second balance and capacitor charge balance under steady state condition [2]:

$$\begin{aligned}
I_s = I_{L1} &= \frac{V_s \times D_{34}}{R_o(1-D_{12})}, \quad I_o = I_{L2} - I_{C2} = \frac{V_o}{R_o},\\
V_{C1} &= \frac{V_s}{(1-D_{12})}, \quad V_{Cd} = \frac{V_s}{(1-D_{12})}, \quad V_o = \frac{V_s \times D_{34}}{(1-D_{12})} = V_{C1} \times D_{34}.
\end{aligned} \tag{3}$$

The steady state equation obtained in (3) can also be obtained by equating the derivatives to zero in (2); the dc equivalent model representing the steady state parameters is shown in Fig. 5b. From (3) a unified voltage conversion ratio is defined as follows.

$$K(D_{12}, D_{34}) = \frac{V_o}{V_s} = \frac{D_{34}}{(1-D_{12})}. \tag{4}$$

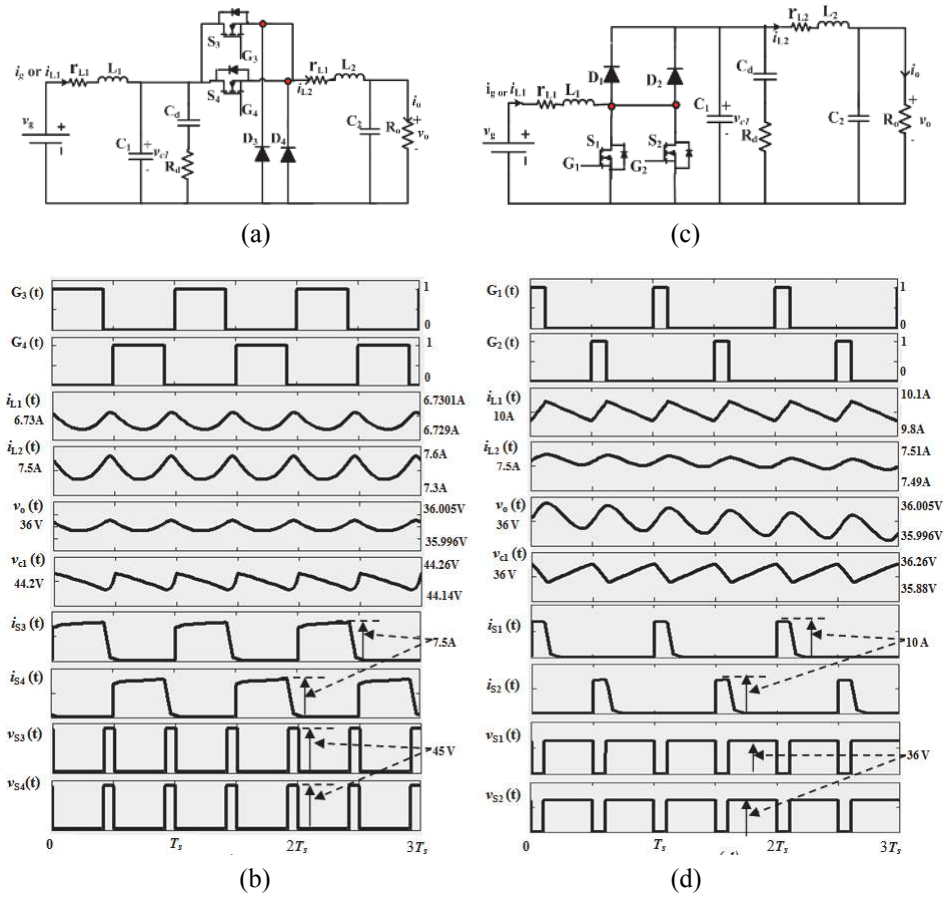


Fig. 3 – *Equivalent circuit and key waveforms in buck and boost operating modes: a) Buck mode equivalent circuit; b) Voltages and currents in buck mode with V_s = 45 V (d_{34} = 0.4185); c) Boost mode equivalent circuit; d) Voltages and currents in boost mode with V_s = 28 V (d_{12} = 0.1388).*

The ultimate objective of the proposed converter is to operate in both buck ($0 < D_{34} < 1$ and $D_{12} = 0$) and boost ($0 < D_{12} < 1$ and $D_{34} = 0$) modes and that the transition from boost to buck and buck to boost modes must occur smoothly.

Let 'u' be the single control variable ranges from 0 to 2. The duty cycles can be re written as

$$D_{12} = \max(0, u-1), \tag{5}$$

$$D_{34} = \min(1, u). \tag{6}$$

With the above consideration of single variable parameter the new voltage conversion ratio results as follows:

$$K(u)=\frac{\min(1,u)}{1-\max(0,u-1)} \quad . \tag{7}$$

Using (7) smooth transition of DC voltage conversion ratio between buck and boost modes of operation can be easily achieved as illustrated in Fig. 5c.

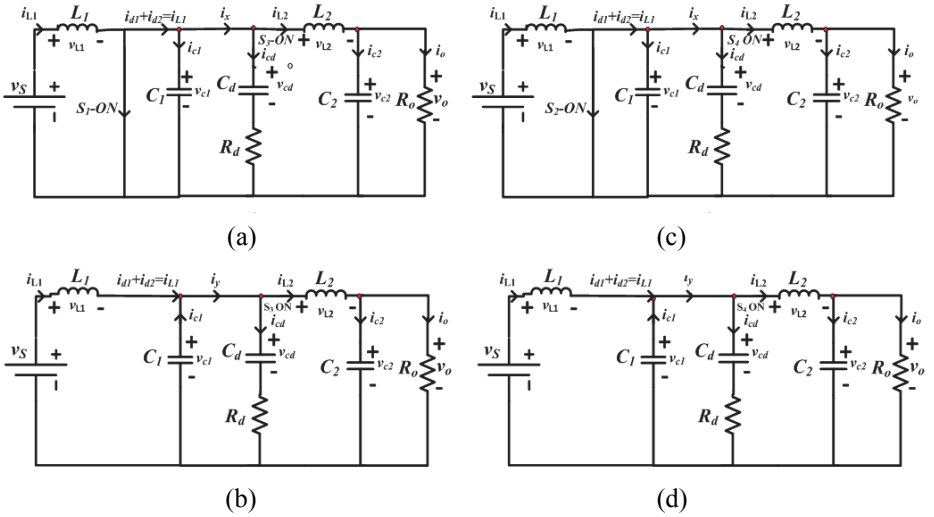


Fig. 4 – *Equivalent circuit diagrams of proposed converter for duty cycle* $d_{12} = 0.1$ *and* $d_{34} = 0.5$*: a) Electrical equivalent circuit diagram for Mode I:* $t_o \le t \le t_1$*; b) Electrical equivalent circuit diagram for Mode II:* $t_1 \le t \le t_2$*; c) Electrical equivalent circuit diagram for Mode III:* $t_2 \le t \le t_3$*; d) Electrical equivalent circuit diagram for Mode IV:* $t_3 \le t \le t_4$.

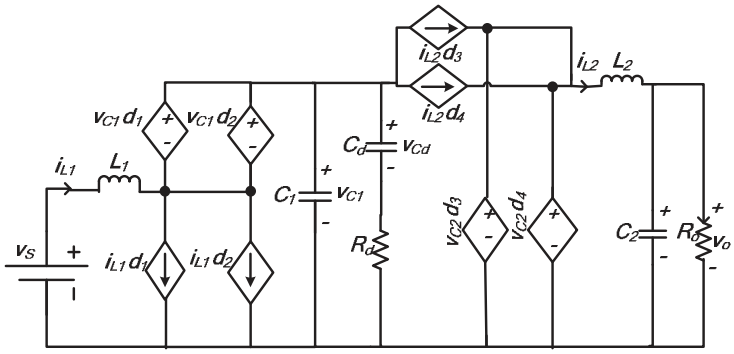
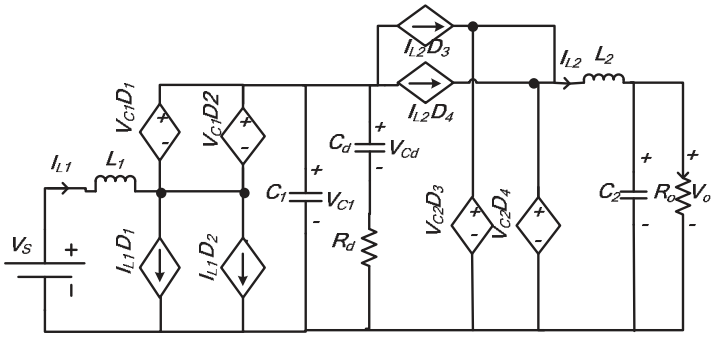
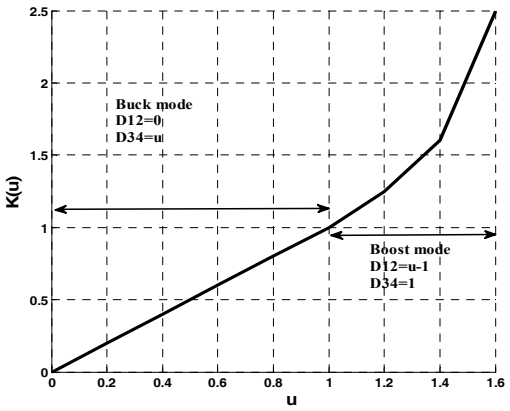


Fig. 5a – *Circuit model of the MDBBC with damping network and DC conversion ratio: a) Equivalent averaged model for large signal analysis;*



(b)



(c)

Fig. 5 – *Circuit model of the MDBBC with damping network and DC conversion ratio: b) Equivalent dc model; c) DC voltage conversion ratio K (u) of MDBBC.*

4 Design Guidelines

The proposed MDBBC is designed as the battery charging /discharging regulator for the 36 V battery bank series, whose design specifications are shown in the **Table 1**. The input voltage ranges from 28 to 45 V and the regulated output voltage is around 36 V. A low ripple current on the input side is the key requirement, and the inductors play major role in reducing the ripple, hence a suitable value of inductance has to be chosen. The current ripple in the both buck and boost side inductors Δi_{L1} and Δi_{L2} is limited to 0.4 A, and then according to that the necessary value of inductance is determined using the equations presented in **Table 2**. Similarly the filter capacitors on both sides are chosen by defining the voltage ripples Δv_{c1} and Δv_{c2} to be maximum 0.2 V, and accordingly the capacitor values are selected.

Table 1
Design specifications for which the converter is designed.

Parameter/Component	Value
Input voltage range	28-45(suits forFCS1000)
Output voltage	36 V
Maximum output power	270 W
Load resistance	4.8 Ω
Switching frequency	50 kHz
Input ripple- peak-peak	0.4 A
Capacitor voltage ripple	0.2 V
Power loss in the damping resistor	1 W

The multi device operation of buck-boost converter helps in using the smaller inductor for reduced ripple current; the inductor value gets reduced by '*q*' times as that of conventional BBC, where *q* is equal to 2 for MDBBC. As discussed in the introduction part about the non-minimum phase system, to overcome this problem a RC damping network is connected at the boundary between buck and boost operating modes. The derived expressions used for selecting these values are presented in **Table 2** as well. After performing the suitable analyses in both buck and boost modes of operation of MDBBC, the finalized list of components are presented in **Table 3**.

Table 2
Necessary equations to determine the parameters of MDBBC.

Buck mode	Boost mode
$L_2 = \frac{(V_s - V_o)V_o}{q \times V_s \times \Delta i_{L2\,Pk-Pk}} \times T_s$	$L_1 = \frac{(V_o - V_s)V_s}{q \times V_o \times \Delta i_{L1\,Pk-Pk}} \times T_s$
$C_2 = \frac{(V_s - V_o)V_o^2}{q \times R \times V_s^2 \times \Delta v_{C2\,Pk-Pk}} \times T_s$	$C_1 = \frac{(V_o - V_s)V_s^2}{q \times R \times V_o^2 \times \Delta v_{C1\,Pk-Pk}} \times T_s$
$C_d > 8C_1, \quad R_d > 0.65\sqrt{\frac{L_1}{C_1}}$	

During buck mode of operation of MDBBC, the passive component parameters are selected based on the following parameters

Input voltage of the converter V_s = 45 V, Output voltage of the converter V_o = 36 V, No. of devices/phase 'q' = 2, allowed ripple current in buck inductor $\Delta i_{L2\,p\text{-}p}$ = 0.6 A, allowed ripple voltage in output capacitor or buck capacitor

$\Delta V_{c2\ pk\text{-}pk}$ = 0.2 V, Switching frequency F_s = 50 kHz. Time period for one cycle T_s = 1/50 kHz = 20 μs.

The passive component values are calculated using the relations given in **Table 2**. The buck inductance L_2 and capacitance C_2 are calculated as:

$$L_2 = \frac{(45-36)36}{2\times 45\times 0.6}\times 20\times 10^{-6}, \quad C_2 = \frac{(45-36)36^2}{2\times 4.8\times 45^2\times 0.2}\times 20\times 10^{-6},$$
$$L_2 = 120\ \mu\text{H}, \qquad C_2 = 60\ \mu\text{F}.$$

The practical values of the components connected in circuit are L_2 = 120 μH and C_2 = 68 F (next higher rating available in market). Also the ripple current in the buck inductor is not considered as important as that of the ripple current in boost inductor, because the load current ripple with 8% is considerable.

During boost mode of operation the passive component parameters are chosen by the following calculations.

Input voltage of the converter V_s = 28 V, Output voltage of the converter V_o = 36 V, No. of devices/phase 'q' = 2, allowed ripple current in buck inductor $\Delta i_{L2\ p\text{-}p}$ = 0.4 A, allowed ripple voltage in output capacitor or buck capacitor $\Delta V_{c2\ pk\text{-}pk}$ = 0.35 V, Switching frequency F_s = 50 kHz, Time period for one cycle T_s = 1/50 kHz = 20 μs.

The passive component values are calculated using the relations given in **Table 2**. The buck inductance L_1 and capacitance C_1 are calculated as:

$$L_1 = \frac{(36-28)28}{2\times 36\times 0.4}\times 20\times 10^{-6}, \quad C_1 = \frac{(36-28)28^2}{2\times 4.8\times 36^2\times 0.35}\times 20\times 10^{-6},$$
$$L_1 = 155\ \mu\text{H}, \qquad L_1 = 28.8\ \mu\text{F}.$$

Apart from the passive components, the damping resistor and capacitor values are chosen based on the condition that the C_d should be greater than eight times of the boost inductor, i.e., 8×47μF = 376 μF. here in the prototype model a capacitor value of 470 μF. The damping resistor value as given in the **Table 2** value is chosen as 1 Ω and around 1 W of heat dissipates in it.

The N-channel MOSFETS with low on-state resistance is considered to achieve good efficiency, and to ensure the faster operation Schottkey diodes are preferred. The inductors are of handmade, the buck side inductor L_2 has to carry 7.5 A and hence SWG 14 wire size is chosen as it can carry a maximum current of 9.3A, whereas on boost side the maximum current flow is 10 A and hence SWG 13 wire is selected as it can carry 12 A easily. Available laboratory type DC voltage sources in conventional lab are not capable of delivering more than 7 A, but the peak current supply requirement is of 10 A under the boost operating mode of the converter, for which a single phase bridge rectifier is preferred to get the required DC voltages for experimentation and measuring of the efficiency.

5 Simulation Study

The proposed converter model is developed and studied on the Matlab/Simulink platform as shown in Fig. 7. All the component values are shown in **Table 3**.

Table 3
Details of the components connected in MDBBC.

Component	Description	Type
S_1, S_2, S_3, S_4	Power MOSFETs	IRFZ44N
D_1, D_2, D_3, D_4	Schottkey diodes	MBR14100
L_1	Boost inductor	Wire size: SWG 13 Core type: Soft ferrite No of turns:20 160 µH
L_2	Buck inductor	Wire size: SWG 14 Core type: Soft ferrite No of turns:15 120 µH
C_1	Ceramic capacitors	47 µF, 63 V
C_d	Damping capacitor	470 µF, 63 V
R_d	Damping Resistor	1 Ω, 1 W
C_2	Output capacitor buck side	68 µF, 100 V

The converter is operated individually in buck and boost operating modes. When operated in buck mode the boost switches S_1 and S_2 are turned off and buck switches S_3 and S_4 are operated in PWM. On the other hand when the converter is operated in boost mode the buck switches are permanently on and the boost switches are operated in PWM. The PWM pulses for the switches are adjusted to get $v_o = 36$ V, this is achieved in buck mode for the duty cycle of $d_{34} = 0.4185$, being the source voltage fixed at 45 V. In boost operating $d_{12} = 0.1388$ for the input voltage of 28 V. As the on time is reduced, the switch conducts for lesser time, reducing the switch conduction. This helps in transferring more input energy to load, thereby increasing efficiency.

Figs. 3b and 3d illustrate the activation signals for buck and boost switches respectively. In order to get voltage regulation the converter can be operated in closed loop voltage controlled mode by a PI controller. Figs. 6a and 6b show the ripples in output inductor current, output current, output voltage and boost capacitor voltage for $v_s = 45$ V and $v_s = 40$ V respectively, which it is observed that for reduced input voltage the inductor ripple current is also reduced by a significant value, it is to be noted that the ripples in input side current during buck mode is very small and one can observe in Fig. 3b.

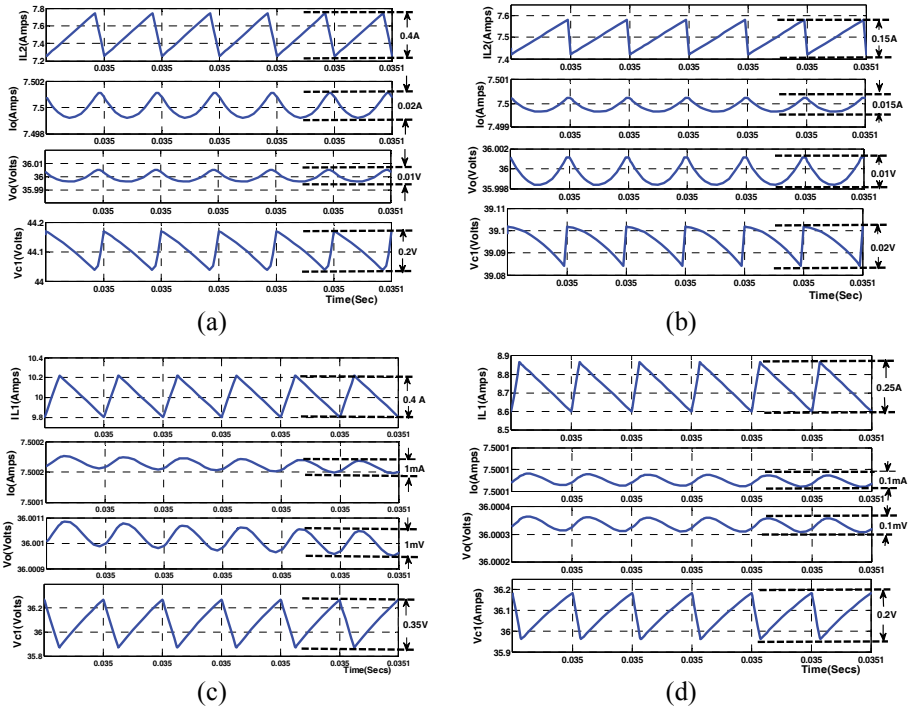


Fig. 6 – *Voltage and current waveforms with ripple in buck and boost operating modes: a) Ripples in current and voltage in buck mode for V_s = 45 V; b) Ripples in current and voltage in buck mode for V_s = 40 V; c) Ripples in I/O current, capacitor voltage and output voltage in boost mode for V_s = 28 V; d) Ripples in I/O current, capacitor voltage and output voltage in boost mode for V_s=32V.*

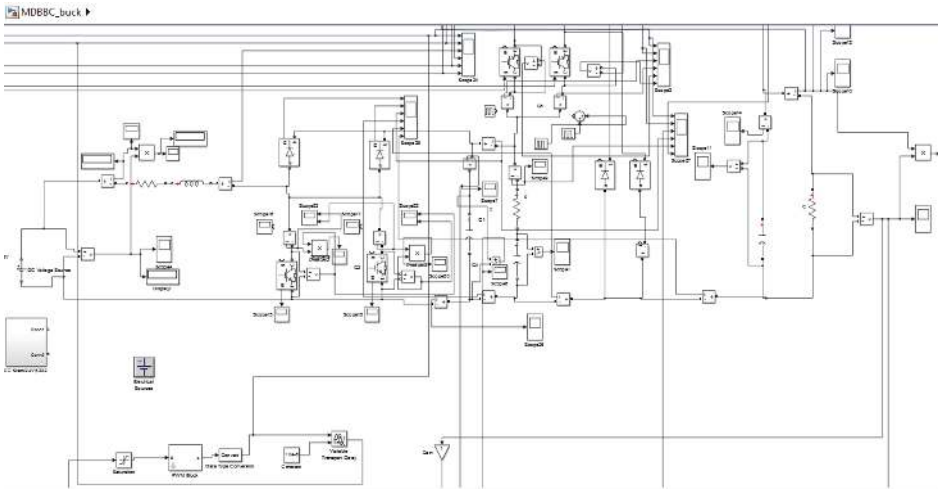


Fig. 7 – *MATLAB Simulation model of the proposed converter.*

Similarly in boost operating mode for two different input voltages v_s = 28 V and v_s = 32 V, the ripples in input current (I_{L1}), output current (I_o) output voltage (V_o) and capacitor C_1 voltage (V_{c1}) are shown in Figs. 6b and 6d.

6 Experimental Results

The proposed MDBBC circuit model is designed to provide an output voltage of 36 V when its source voltage varies from 28 to 45 V. The experimental setup and prototype model is shown in in Fig. 8. The maximum power is restricted to 270 W (36V×7.5 A) or (7.5^2×4.8 Ω) and the corresponding load resistance is 4.8 Ω. The duty cycles for the buck mode is in the range of $0.4185 < D_{34} < 1$ and for boost mode is $0 < D_1 < 0.1388$. The switching frequency is selected to be of 50 kHz, as this is the optimum frequency level which is observed for the proposed converter. The frequency over the 50 kHz introduces additional switching and conduction losses but the passive components sizes get reduced, the increased losses leads to the less energy efficient system. Choosing below the 50 kHz is also not feasible requires large size passive components and hence it is selected based on the trade-off among the power losses, size of passive components and EMI interference.

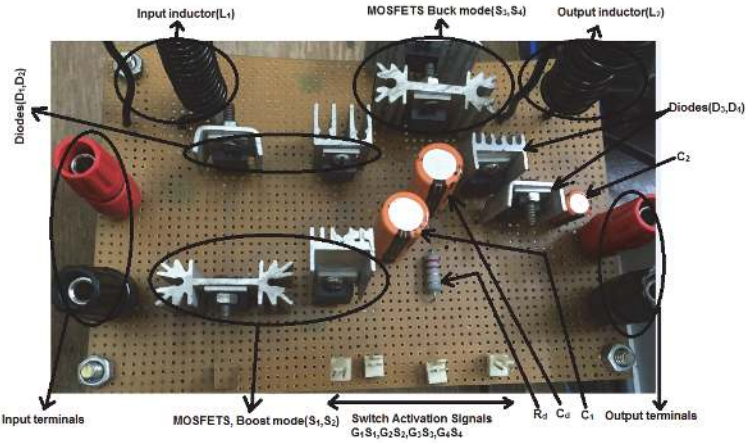
Further the inductor ripple current and capacitor voltage ripple are selected to be of 0.4 A and 0.2 V respectively, provided the passive components to be of less value as shown in **Table 3**. The proposed converter can be best suitable as FC voltage regulation system to meet the practical application as voltage regulator for a Horizon PEM fuel cell model "*H-1000-FCS-C1000"*. Its voltage varies from 28 to 45 V full load to no load. The output voltage of this FC is unregulated and it has to be regulated to get 36 V constant values for the purpose of charging a 36V battery bank. The components are designed based on the expressions and aforementioned ripple as shown in **Table 2** and **Table 1**.

To obtain the real time switching signals for the buck and boost switches an *"Altium3000NB"* FPGA controller has been used. A triangle shaped carrier wave is compared with the reference DC voltage to produce the firing pulses by using *Xylinx Spartan ISE 14.1* system generator, which can convert the PWM logic into high speed *VHDL* code. The generated code is dumped into the "*Altium3000NB FPGA"*. Further the generated pulses from the *FPGA* ports are given to the driver circuits of the switches. The key experimental waveforms are obtained on the DSO.

The waveforms illustrated here are of gating pulses for the switches as shown in Figs. 9a, 9b and 9c show the ripple current on the input side during the boost operation mode, because the key point of interest is the reduction of ripple current. The ripple current observed is close to the simulation results shown in the Figs. 6c and 6d, being 4%, which is highly appreciable for fuel cell applications. The previous reported value of the input ripple current by several authors are 5.2% in [20] and 9.2% in [30], 23% in [29], 28% in [19], 32% in [15], and 33% in [28].

For any power converter the energy conversion efficiency is an important consideration, the proposed converter efficiency is determined by experimental setup which includes power analyser and dc electronic load, the measured efficiency includes the control stages and driver stage power losses, calibrated shunt resistors are used to measure the currents on input and output side. Fig. 10 shows the overall system efficiency as a function of load or output current i_o for different source voltage levels and the variation of efficiency is plotted for different output currents and source voltage as reference on the horizontal axis. One can see from the efficiency plot that the maximum efficacy occurs at the end of the buck mode of operation, i.e., v_s = 42 V – 44 V.

(a)



(b)

Fig. 8 – *Experimental setup and power circuit of MDBBC: a) Experimental setup; b) Power circuit.*

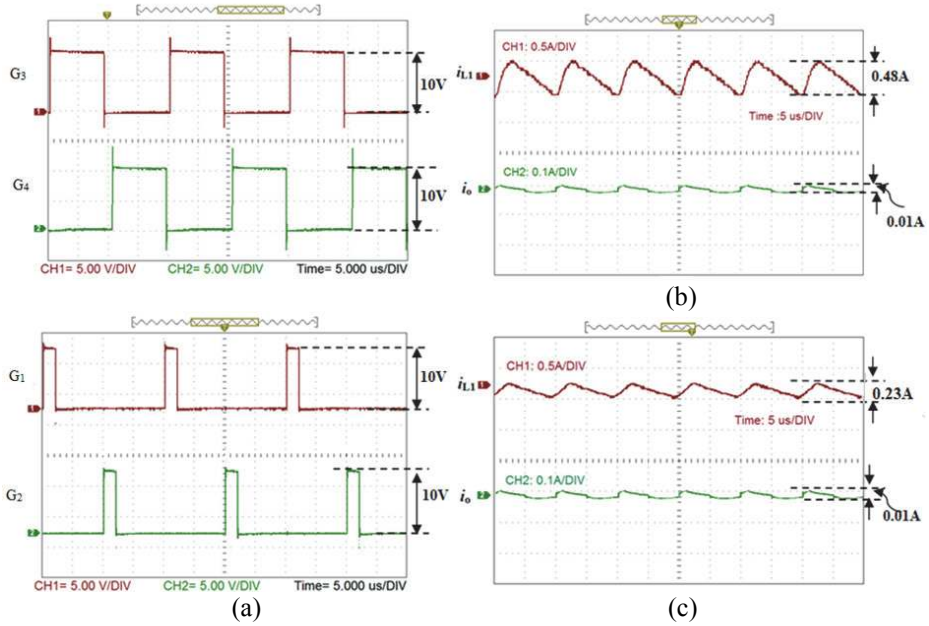


Fig. 9 – *Experimental results of MDBBC prototype converter model: a) Switching activation signals for buck and boost mode switches; b) Input source current or inductor* (L_1) *current and output load current ripples in boost operating mode for* V_s = 28 V; *c) Input source current or inductor* (L_1) *current and output load current ripples in boost operating mode for* V_s = 32 V.

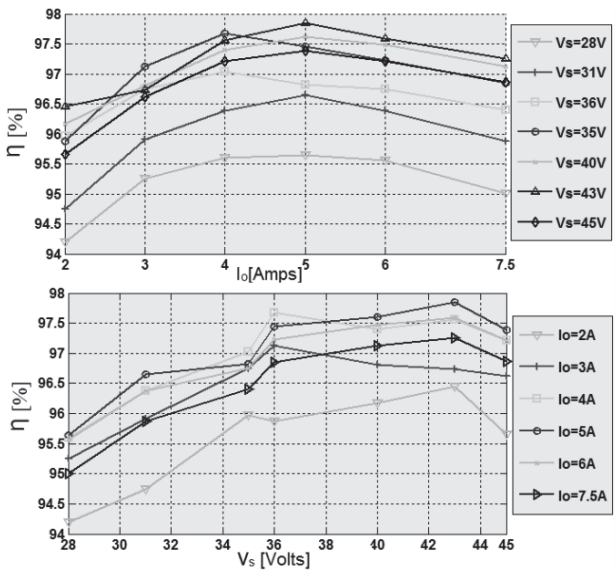


Fig. 10 – *Measured efficiency of the proposed MDBBC for* v_o = 36V.

It can also be seen from energy efficiency plot that when the converter is operating in the buck stage, the efficiency obtained is higher compared to the boost stage, the reason for this is the boost switches are off during the buck mode of operation, and hence the power losses reduce. Thus such high value of efficiency with hard switching operation proves that the proposed converter is best suitable for low voltage applications. The overall maximum power stage losses which occur in the process of operation are of 18 W with inclusion of power losses in the inductor. These losses can be further reduced by employing some zero voltage switching, multi device interleaving operation.

7 Conclusion

A new non inverting multi device buck-boost dc-dc converter suitable for fuel cell low voltage applications has been introduced in this paper. The designed MDBBC operates either in buck or boost CCM mode and the converter behaviour under steady state operation are presented. The converter efficiently operates in buck and boost operating modes, when operating in buck mode the boost switches are off whereas in boost operation the buck switches are permanently on. The placement of an intermediate damping network between the buck and boost operating modes reduces the damping oscillation in the output voltage under boundary operation. Further the basic circuit operation of proposed converter, design procedures and selection of key components were clearly described with neat diagrams. Moreover the *s* domain model and analysis of converter differential equations are derived.

A high efficiency is obtained under the three operating modes of operation including buck, boost and boundary region operation, based on the I/O voltage ratio factor. It has been experimentally verified that the proposed MDBBC has peak and average efficiency of 97.68% and 96.25% respectively, which can be further improved by ZVS or multi device interleaving operation on the boost side or input side of the converter. The designed converter is best suitable for the applications such as FC devices for battery charging because it has the ripple current less than the permissible value as 5% and other applications such as PV panels, super capacitors and other low voltage applications also can use this topology. Further, operating the converter in buck-boost mode results in a non-minimum phase system as there is presence of RHP zeros on the *s-plane*, research yet to carry to overcome the drawback of non-minimum phase system.

8 Acknowledgment

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9 Appendix

In this appendix the differential equations of capacitor voltages and currents for the equivalent circuits shown in Figs. 4c – 4d.

(b) Mode II: $t_1 \le t \le t_2$, Fig. 4b

$$\begin{aligned}
v_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} = v_s(t) - v_{c1}(t), \\
v_{L2}(t) &= L_2 \frac{di_{L2}(t)}{dt} = v_{cd}(t) - v_o(t) or v_{c1}(t) - v_o(t), \\
i_{c1}(t) &= C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) - (i_{cd}(t) + i_{L2}(t)) or i_{L1}(t) - i_y(t), \\
i_{cd}(t) &= C_d \frac{dvc_d(t)}{dt} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d} = i_y(t) - i_{L2}(t).
\end{aligned} \tag{A1}$$

Here i_y is transition mode current, the current between two operating modes:

$$i_y = i_{cd}(t) + i_{L2}(t) \text{ or } i_{c1}(t) + i_{L1}(t),$$

$$i_{c2}(t) = C_2 \frac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} = i_{L2}(t) - \frac{v_o(t)}{R_o}.$$

(c) Mode III: $t_2 \le t \le t_3$, Fig. 4c

$$\begin{aligned}
v_{L1}(t) &= L_1 \frac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} = v_s(t) - v_{c1}(t), \\
v_{L2}(t) &= L_2 \frac{\mathrm{d}i_{L2}(t)}{dt} = v_{cd}(t) - v_o(t) \quad \text{or} \quad v_{c1}(t) - v_o(t), \\
i_{c1}(t) &= C_1 \frac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} = i_{L1}(t) - \left(i_{cd}(t) + i_{L2}(t)\right), \\
i_{cd}(t) &= C_d \frac{\mathrm{d}vc_d(t)}{\mathrm{d}t} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d} = i_x(t) - i_{L2}(t).
\end{aligned} \tag{A2}$$

Here i_x is transition mode current, the current between two operating modes:

$$i_x = i_c(t) + i_{L2}(t) \text{ or } i_{L1}(t) - i_{c1}(t),$$

$$i_{c2}(t) = C_2 \frac{\mathrm{d}v_{C2}(t)}{\mathrm{d}t} = i_{L2}(t) - \frac{v_o(t)}{R_o}.$$

(d) Mode IV: $t_3 \le t \le t_4$, Fig. 4d

$$\begin{aligned} v_{L1}(t) &= L_1 \frac{\mathrm{d}\, i_{L1}(t)}{\mathrm{d}\, t} = v_s(t) - v_{c1}(t), \\ v_{L2}(t) &= L_2 \frac{\mathrm{d}\, i_{L2}(t)}{\mathrm{d}\, t} = v_{cd}(t) - v_o(t) \quad \text{or} \quad v_{c1}(t) - v_o(t), \\ i_{c1}(t) &= C_1 \frac{\mathrm{d}\, v_{C1}(t)}{\mathrm{d}\, t} = i_{L1}(t) - \left(i_{cd}(t) + i_{L2}(t)\right) \quad \text{or} \quad i_{L1}(t) - i_y(t), \\ i_{cd}(t) &= C_d \frac{\mathrm{d}\, vc_d(t)}{\mathrm{d}\, t} = \frac{v_{c1}(t) - v_{cd}(t)}{R_d}(t) = i_y(t) - i_{L2}(t). \end{aligned} \tag{A3}$$

Here i_y is transition mode current, the current between two operating modes:

$$i_y = i_{cd}(t) + i_{L2}(t) \text{ or } i_{c1}(t) + i_{L1}(t)$$

$$i_{c2}(t) = C_2 \frac{dv_{C2}(t)}{dt} = i_{L2}(t) - \frac{v_o(t)}{R_o}.$$

10 References

[1] L. Palma, P. Enjeti.: A Modular Fuel Cell, Modular DC–DC Converter Concept for High Performance and Enhanced Reliability, IEEE Transactions on Power Electronics, Vol. 24, No. 6, 2009, pp. 1437 – 1443.

[2] R. W. Erickson, D. Maksimovic: Fundamentals of Power Electronics, 2nd edition, Kluwer Academic, New York, 2001.

[3] P. W. Lee, Y. S. Lee, D. K.W. Cheng, X. C. Liu.: Steady-State Analysis of an Interleaved Boost Converter with Coupled Inductors, IEEE Transactions on Industrial Electronics, Vol. 47, No. 4, 2000, pp. 787 – 795.

[4] B. R. Lin, H. H. Lu.: A Novel PWM Scheme for Single-Phase Three- Level Power-Factor-Correction Circuit, IEEE Transactions on Industrial Electronics, Vol. 47, No. 2, 2000, pp. 245 – 252.

[5] D. Maksimovic, R. Erickson: Universal-Input, High-Power-Factor, Boost Doubler Rectifiers, Applied Power Electronics Conference and Exposition, APEC'95, Dallas, USA, 5 – 9 March 1995,Conference Proceedings, Vol. 1, 1995, pp. 459 – 465.

[6] J. Chen, D. Maksimovic, R. Erickson: Buck-Boost PWM Converters Having Two Independently Controlled Switches, 32nd IEEE Annual Power Electronics Specialists Conference, PESC 2001, Vancouver, Canada, 17 – 21 June 2001, Vol. 2, pp. 736 – 741.

[7] M. Gaboriault, A. Notman.: A High Efficiency, Non-Inverting, Buck boost DC-DC Converter, Applied Power Electronics Conference and Exposition, APEC 2004, 19th Annual IEEE, Anaheim, CA, USA, 22 – 26 February 2004, Vol. 3, 2004, pp. 1411 – 1415.

[8] P. C. Huang, W. Q. Wu, H. H. Ho, K. H. Chen: Hybrid Buck-Boost Feedforward and Reduced Average Inductor Current Techniques in Fast Line Transient and High-Efficiency Buck-Boost Converter, IEEE Transactions on Power Electronics, Vol. 25, No. 3, 2010, pp. 719 – 730.

[9] B. Sahu, G. A. Rincon-Mora: A Low Voltage, Dynamic, Noninverting, Synchronous Buck-Boost Converter for Portable Applications, IEEE Transactions on Power Electronics, Vol. 19, No. 2, 2004, pp. 443 – 452.

[10] Y. J. Lee, A. Khaligh, A. Emadi: A Compensation Technique for Smooth Transitions in a Noninverting Buck-Boost Converter, IEEE Transactions on Power Electronics, Vol. 24, No. 4, 2009, pp. 1002 – 1015.

[11] Y. J. Lee, A. Khaligh, A. Chakraborty, A. Emadi: Digital Combination of Buck and Boost Converters to Control a Positive Buck-Boost Converter and Improve the Output Transients, IEEE Transactions on Power Electronics, Vol. 24, No. 5, 2009, pp. 1267 – 1279.

[12] D. Biel, F. Guinjoan, E. Fossas, J. Chavarria: Sliding-Mode Control Design of a Boost-Buck Switching Converter for AC Signal Generation, IEEE Transactions on Circuits and Systems I, Vol. 51, No. 8, 2004, pp. 1539 – 1551.

[13] J. Chen, D. Maksimovic, R. W. Erickson: Analysis and Design of a Low-Stress Buck-Boost Converter in Universal-Input PFC Applications, IEEE Transactions on Power Electronics, Vol. 21, No. 2, 2006, pp. 320 – 329.

[14] T. Crocker, N. Cooper: Fast and Furious [Electric Dreams], Power Engineer, Vol. 18, No. 4, 2004, pp. 39 – 41.

[15] C. Restrepo, J. Calvente, A. Cid-Pastor, A. E. Aroudi, R. Giral: A Noninverting Buck-Boost DC-DC Switching Converter with High Efficiency and Wide Bandwidth, IEEE Transactions on Power Electronics, Vol. 26, No. 9, 2011, pp. 2490 – 2503.

[16] M. He, F. Zhang, J. Xu, P. Yang, T. Yan: High-Efficiency Two-Switch Tri-State Buck–Boost Power Factor Correction Converter with Fast Dynamic Response and Low-Inductor Current Ripple, IET Power Electronics, Vol. 6, No. 8, 2013, pp. 1544 – 1554.

[17] D. Ma, W. H. Ki: Fast-Transient PCCM Switching Converter with Freewheel Switching Control, IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 54, No. 9, 2007, pp. 825 – 829.

[18] K. Viswanathan, R. Oruganti, D. Srinivasan: Dual-Mode Control of Tri-State Boost Converter for Improved Performance, IEEE Transactions on Power Electronics, Vol. 20, No. 4, 2005, pp. 790 – 797.

[19] H. K. Liao, T. J. Liang, L. S. Yang, J. F. Chen: Non-Inverting Buck–Boost Converter with Interleaved Technique for Fuel-Cell System, IET Power Electronics, Vol. 5, No. 8, 2012, pp. 1379 – 1388.

[20] V. Samavatian, A. Radan: A Novel Low-Ripple Interleaved Buck-Boost Converter with High Efficiency and Low Oscillations for Fuel Cell Applications, International Journal of Electrical Power and Energy Systems, Vol. 63, 2014, pp. 446 – 454.

[21] Y. J. Lee, A. Emadi: Phase Shift Switching SCheme for DC/DC Boost Converter with Switches in Parallel, IEEE Vehicle Power Propulsion Conference, VPPC'08, Harbin, China, 3 – 5 September 2008, Conference Proceedings, pp. 1 – 6.

[22] R. S. Gemmen: Analysis for the Effect of Inverter Ripple Current on Fuel Cell Operating Condition, Journal of Fluids Engineering, Transactions of the ASME, Vol. 125, No. 3, 2003, pp. 576 – 585.

[23] W. Choi, P. N. Enjeti, J. W. Howze, G. Joung: An Experimental Evaluation of the Effects of Ripple Current Generated by the Power Conditioning Stage on a Proton Exchange Membrane Fuel Cell Stack, Journal of Materials Engineering and Performance, Vol. 13, No 3, 2004, pp. 257 – 264.

[24] J. Calvente, L. Martinez-Salamero, P. Garces, A. Romero: Zero Dynamics-Based Design of Damping Networks for Switching Converters, IEEE Transactions on Aerospace and Electronic Systems, Vol. 39, No. 4, 2003, pp. 1292 – 1303.

[25] M. Veerachary: General Rules for Signal Flow Graph Modeling and Analysis of DC–DC Converters, IEEE Transactions on Aerospace and Electronic Systems, Vol. 40, No. 1, 2004, pp. 259 – 271.

[26] E. Van Dijk, J. N. Spruijt, D. M. O'Sullivan, J. B. Klaassens: Pwm-Switch Modeling of DC-DC Converters, IEEE Transactions on Power Electronics, Vol. 10, No. 6, 1995, pp. 659 – 665.

[27] K. I. Hwu, T. J. Peng: A Novel Buck-Boost Converter Combining KY and Buck Converters, IEEE Transactions on Power Electronics, Vol. 27, No. 5, 2012, pp. 2236 – 2241.

[28] J. M. Blanes, R. Gutierrez, A. Garrigos, J.L. Lizan, J. Martinez Cuadrado: Electric Vehicle Battery Life Extension Using Ultracapacitors and an FPGA Controlled Interleaved Buck–Boost Converter, IEEE Transactions on Power Electronics, Vol. 28, No. 12, 2013, pp. 5940 – 5948.

[29] V. Samavatian, A. Radan: A High Efficiency Input/Output Magnetically Coupled Interleaved Buck–Boost Converter with Low Internal Oscillation for Fuel-Cell Applications: CCM Steady-State Analysis, IEEE Transactions on Industrial Electronics, Vol. 62, No. 9, 2015, pp. 5560 – 5568.

[30] M. Venkatesh Naik, P. Samuel: Analysis of Ripple Current, Power Losses and High Efficiency of Dc–Dc Converters for Fuel Cell Power Generating Systems, Renewable And Sustainable Energy Reviews, Vol. 59, 2016, pp. 1080 – 1088.