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A Novel High Efficiency CMOS RF/DC Power Harvester Based on Constant ON/OFF Time Buck Controller for 60GHz Frequency Band

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Abstract: A novel 60 GHz RF/DC power harvesting system is presented. The system consists of RF to DC rectifier and a DC/DC Buck converter based on constant ON/OFF time (COOT) control. The rectifier has a structure of voltage doubler, but employs diodes that have lower parasitics compared to those of the standard MOSFET diodes, resulting in improved power conversion efficiency. The peak efficiency of the rectifier obtained with the extracted parasitics for the output power of 1 mW is about 25%. In order to keep the output voltage of the system to 1.2 V, the COOT control in the Buck converter is used. COOT control has much better efficiency at low output powers compared to the PWM systems. For correct operation of the COOT control, auxiliary sub-blocks: a low power high-speed comparator, a hysteresis comparator, and a high-speed voltage reference are designed and presented. The maximum switching frequency in the Buck converter is about 100MHz and the whole control system has very low static power consumption. The efficiency of the overall system for the output power of 1mW is about 21%. The system is designed in 65 nm CMOS technology.

Keywords: 60GHz, CMOS, Power harvesting, Buck converter, Rectifier, Voltage doubler.

1 Introduction

Rapid growth in wireless systems based on ultra-low power radio architectures, from biomedical implants and radio-frequency identifications (RFIDs) to wireless sensor networks (WSNs), is evident nowadays. In such a system the antenna and battery occupy a large area. In order to comply with the small size requirement and to overcome the limited battery life time, the alternative remote power source techniques, such as wireless power transmission, have been considered to build independent, battery-less, ultra low power (ULP) systems. The most challenging issue for the fully integrated solutions is to provide enough power on chip for both the sensor and radio.

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Wireless power transfer at mm-wave frequencies can take advantage of the small wavelength which enables integration of the wireless power receiver together in the CMOS technology. Most of the RF to DC rectifiers is based on Dickson voltage multiplier. Such rectifier is shown in [1] where 10 stages of multipliers are used to convert the 60 GHz RF power to DC which powers-up the RFID tag. The diodes used in this rectifier are having body-drain connections which modulate threshold voltage of the diodes. This is one of the techniques that lower threshold voltage of the diodes which improves the efficiency of the rectifier. Another technique is the input voltage boosting with a series inductor. In [2, 3] a three stage voltage multiplier is used together with a series inductor for rectification. The peak efficiency of 8% at 50GHz is reported in [2], and the rectifier produces 1 V output voltage with -7dBm input power at 52 GHz. In [3] 4.4% efficiency is obtained with 7 dBm input power at 60 GHz when the rectifier is loaded by 1.5kΩ. Another threshold modulation technique is reported in [4] and [5] where the inductor is placed between the gate and drain of a MOSFET. The inductor, together with parasitic capacitances of the MOSFET in resonance, boosts the voltage at the gate, increasing in that way the gate-source voltage. In [4] a peak efficiency of 7% is reported for 1 mA load when the rectifier is excited with -14.5 dBm input power at 62 GHz. For that power level the rectifier produces about 100mV of output voltage. The rectifier in [5], which operates at 71 GHz, has a peak efficiency of 8% when driven with 5dBm input power and when loaded by 0.7 mA. When loaded by 5 MΩ, with 5dBm input power, the rectifier produces about 1V of output voltage. The rectifier reported in [6] operates at 94 GHz and has a peak efficiency of 10%.

One of the main reasons for low efficiency is the influence of parasitics of the MOSFETs which have very significant impact at mm-wave frequencies. In order to improve the efficiency, the rectifier in this work has minimized parasitics. It consists of one stage of voltage multiplier and a series inductor for the input voltage boosting. The diodes in the rectifier have higher threshold voltage than the diodes having body-drain connections, but this is not the problem since a series inductor is used to boost the input voltage enough to excite the rectifier. The rectifier, the parasitics extracted, has an efficiency of 24.8% when driven by 6.2 dBm input power and when loaded by 1.44 kΩ. Output voltage of the rectifier is then 1.2 V resulting in the output power of 1mW. In order to stabilize the output voltage at a desired value for different loads, a DC/DC Buck converter is implemented by using constant ON/OFF time control [7]. Because of 60GHz input signal, the output voltage starts to rise very fast. In order to achieve correct operation of COOT control system, high speed voltage reference of 1μs response is also applied. Efficiency of the overall system (RF/DC rectifier + DC/DC converter) is about 21%.

2 RF/DC rectifier

For the rectifiers which operate at somewhat lower frequencies (e.g. 2.4 GHz) a higher efficiency is achieved by minimizing the MOSFET channel length and by choosing proper channel width which lowers the parasitic resistance of the diodes. When the diodes are off, they have parasitic capacitances which isolate the output voltage. These parasitic capacitances can be neglected at lower frequencies. However, wide transistors have higher parasitic capacitances which have a huge impact on the efficiency at the mm-wave frequencies (e.g. 60 GHz). In other words, at mm-wave frequencies output voltage isolation must be considered while choosing the MOSFET dimensions. In standard diode connected MOSFETs parasitic capacitance between the gate and source has a huge impact on the efficiency and it would be desirable to eliminate that capacitance which is implemented in the diodes used in this work. These diodes formed by NMOS and PMOS transistors are shown in Fig. 1. The gate and source terminal are shorted as well as the gate and drain which significantly minimizes parasitic capacitances. In the NMOS transistor the bulk is p-type which is the anode, and the gate/source/drain terminals are n-type which is the cathode of the diode. Similar applies for the PMOS transistor.

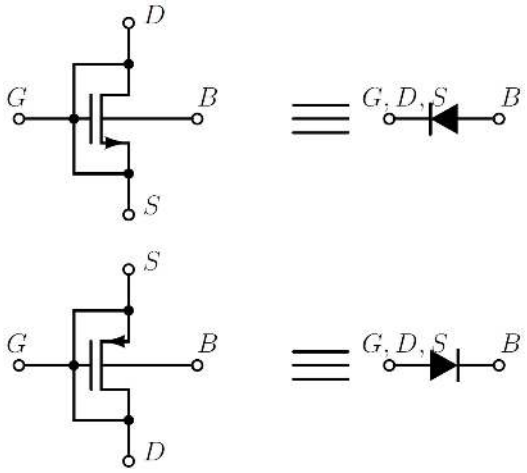

Fig. 1 – *Diodes which are used in RF/DC converter.*

If the transistor has N fingers, then we have N+1 diodes in parallel which lowers the parasitic resistance when the diodes are ON, while the parasitic capacitances are still small. Variation of the parasitic capacitance for different numbers of fingers is shown in Fig. 2. As can be seen, the diodes from this work have smaller parasitic capacitances than the standard diode connected MOSFET. This is because the capacitance between the gate and source/drain, which is the biggest parasitic capacitance, is eliminated. At higher frequencies

this is very important since capacitances of the order of femto Farads have significant impact on the efficiency. Also, in parallel with the parasitic capacitances when the diodes are OFF, we have parasitic resistance which models a finite Q factor of the capacitances. This resistance should be large enough to minimize the losses (ideally this resistance is infinite) and this is shown in Fig. 3. Again, the parasitic resistance is higher than the resistance in the diode connected MOSFET which means that a higher efficiency could be expected with the diodes used in this work.

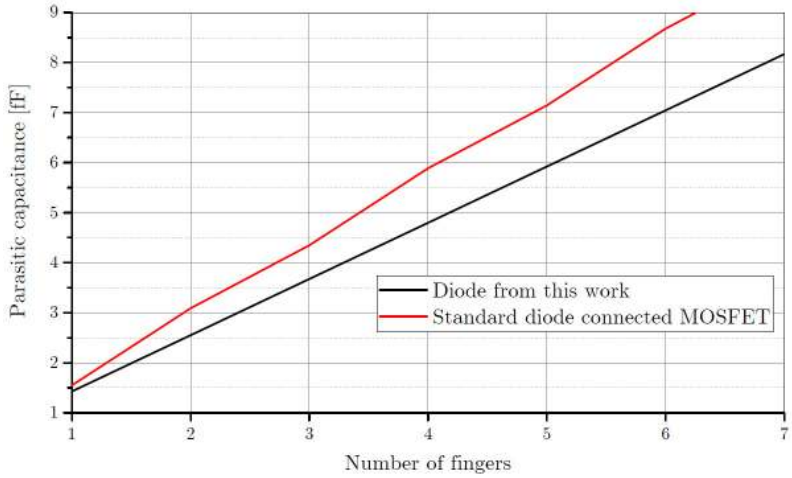

Fig. 2 – *A comparison of the parasitic capacitances of the two types of diodes.*

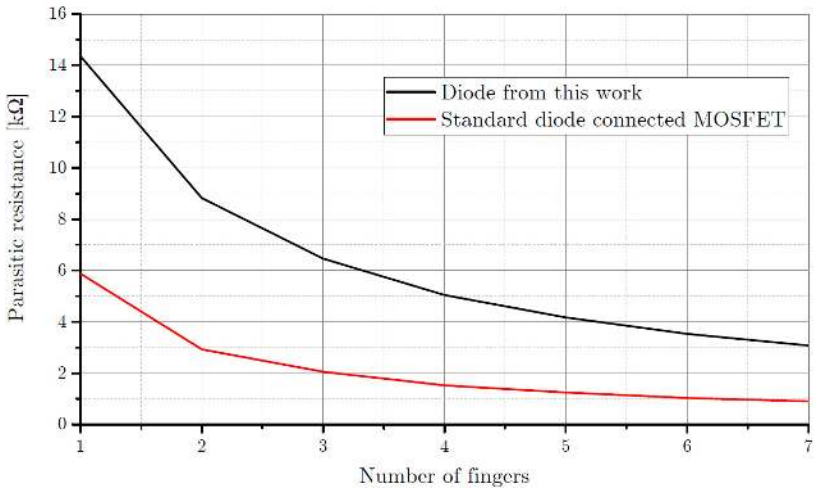

Fig. 3 – *A comparison of the parasitic resistances of the two types of diodes.*

The RF/DC converter used in this work has one stage of Dickson multiplier and is shown in Fig. 4. Inductor L_{in} is used for the input voltage boosting. NMOS transistor M_1 should be in isolated p-type bulk, thus deep-n-well technology is needed to overcome the latch-up problem. Transistors with thicker oxide are used as diode because we expect voltages higher than 1.2 V. Channel lengths for such NMOS and PMOS transistors are 500 nm and 400 nm, respectively, so we choose the minimal length to minimize the parasitic resistances of the diodes. Total widths of both NMOS and PMOS transistors are fixed at 2.4 μm. In order to have several diodes in parallel, as explained earlier, we choose 6 fingers for both transistors which lead to the finger width of 400 nm. This is the compromise between the parasitic resistance and parasitic capacitance of the transistor. We could lower the resistance if we choose wider transistors, but then the parasitic capacitance would be higher which is not desirable. Capacitor C_{in} should be at least 10 times higher than the parasitic capacitances of the converter. In our case C_{in} = 250 fF. If the total parasitic capacitance of the converter is $C_{in\text{-}RFDC}$, then the series inductor can be obtained from:

$$L_{in} = \frac{1}{(2\pi f_0)^2 C_{in-RFDC}}, \tag{1}$$

From the simulations we have obtained $C_{in\text{-}RFDC}$ = 23fF, so the series inductance is L_{in} = 306pH.

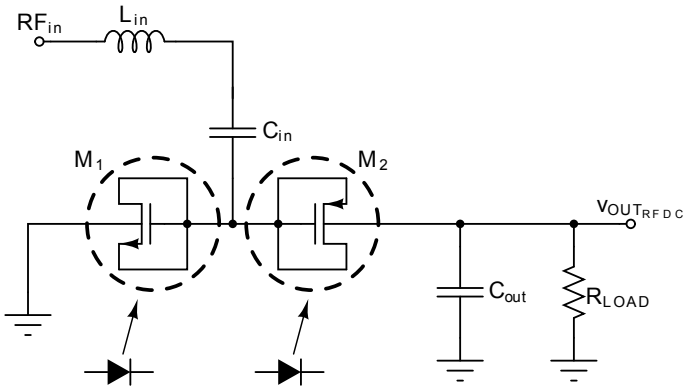

Fig. 4 – *The RF/DC rectifier.*

Layout of the RF/DC rectifier is shown in Fig. 5. At the left side, and the largest part, is series inductor L_{in}. At the right side are input capacitor C_{in} and NMOS and PMOS diodes M_1 and M_2. Decoupling capacitor C_{OUT} is omitted at this time and its capacitance will be obtained at the TOP level of the layout where this capacitor will fill the empty space around the inductors and the other sub-blocks of the system.

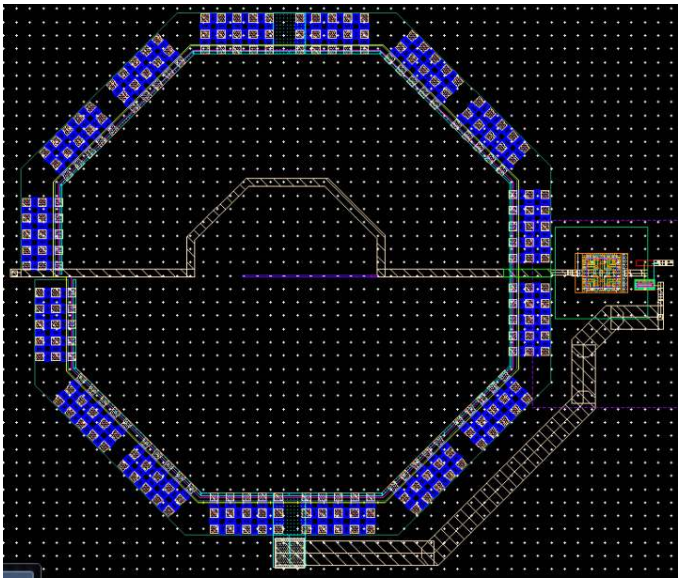

Fig. 5 – *The RF/DC rectifier - layout*.

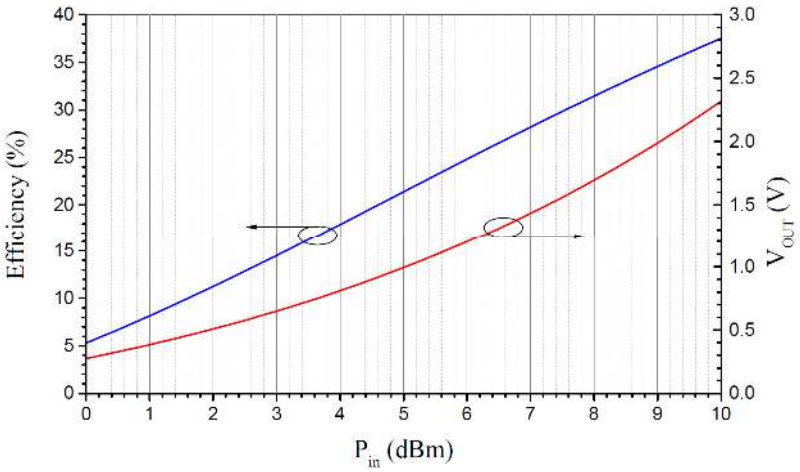

Fig. 6 – *The output voltage and efficiency for different input powers*.

The output voltage and efficiency, for different input powers, are shown in Fig. 6. The load resistance for this simulation is fixed at 1.44 kΩ.

It can be seen that for the input power of 6.2dBm we have the output voltage of 1.2V which results in the output power of 1mW. Thus, the efficiency for this case is about 25%.

3 DC/DC Buck Converter with COOT Control System

In order to keep the output voltage constant, a DC/DC Buck converter including a COOT control system is used. For the light loads the PWM control system suffers from the instability and has a low efficiency. The COOT control system is better for low output loads but the output voltage ripple cannot be kept as low as with the PWM control system. In our case this is not crucial, so the COOT system is implemented as control for the Buck converter and it is shown in Fig. 7 [7].

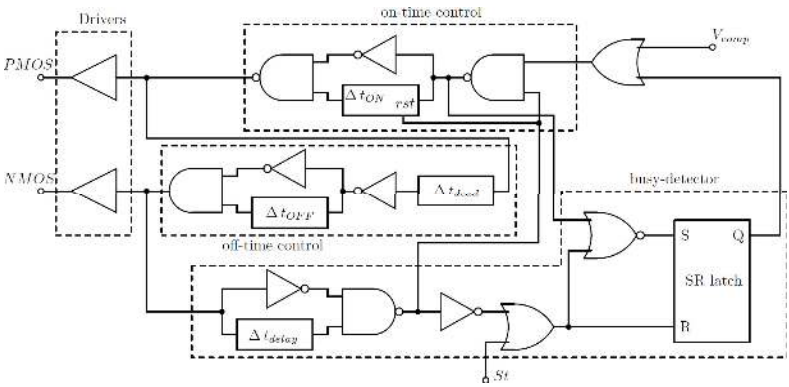

Fig. 7 – *COOT control system*.

The on-time and off-time control consists of a monostable multivibrator which triggers at the falling edge of the input signal. The on-time control generates a low pulse having fixed interval t_{on}, while the off-time control generates a high pulse having fixed interval t_{off}. Because a DC/DC converter will operate in a discontinuous conduction mode (DCM), the input voltage of the Buck converter will not be higher than 2V, t_{on} should be longer than t_{off}. Because we use synchronous Buck converter (will be explained later), t_{off} interval should be very short to discharge the inductor. A delay of duration Δt_{dead} prevents the NMOS transistor of the Buck converter (auxiliary switch) to turn ON while the PMOS transistor of the Buck converter (main switch) is ON. The busy detector prevents the system to start a new cycle while the previous one is not finished. The drivers of the switches are implemented as digital tapered inverters. If the output voltage is below desired level, V_{comp} is at logic 1 and the control system starts the cycle and continues oscillating until the output voltage reaches the desired level. If the output voltage is above the desired level, V_{comp} is at logic 0 and the control system is inactive.

The DC/DC Buck converter the associated control system, and all other sub-blocks are shown in Fig. 8. Inductor L_{OUT} is made of 5.5 turns and has

inductance of about 12.4nH. The PMOS and NMOS switches are of minimal channel length and the widths of 150μm and 10μm, respectively.

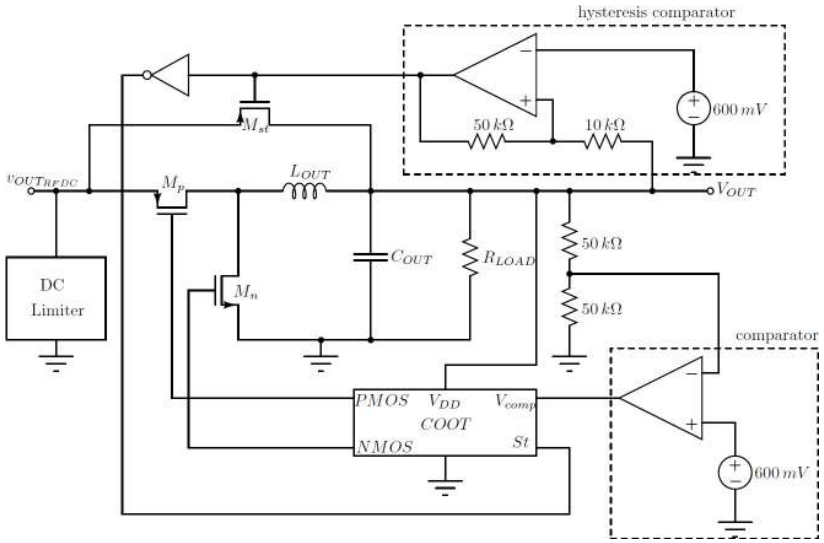

Fig. 8 – *The DC/DC Buck converter and control system*.

Input voltage of the Buck converter is output voltage of the RF/DC rectifier. At the beginning, output voltage of the RF/DC converter starts rising from zero to a higher voltage. The hysteresis comparator is powered from the input of the Buck converter and when this voltage is high enough, the hysteresis comparator closes startup transistor M_{st} and the output voltage of the Buck converter starts rising. COOT control is supplied from the output of the Buck converter and when this voltage is high enough to starts the oscillation, startup transistor M_{st} is opened and COOT takes over the control. It is very important to have the hysteresis comparator whose one threshold voltage is independent of the supply voltage because this threshold voltage determines opening of startup transistor M_{st}. For this purpose the hysteresis comparator from Fig. 9 is used [8]. Transfer function of the comparator is shown in Fig. 10. The higher and lower threshold voltages are given by:

$$V_{TH} = \left(1+\frac{R_2}{R_1}\right)V_{ref} - \frac{R_2}{R_1}V_{OL} \approx \left(1+\frac{R_2}{R_1}\right)V_{ref}\,, \tag{2}$$

$$V_{TL} = \left(1+\frac{R_2}{R_1}\right)V_{ref} - \frac{R_2}{R_1}V_{OH}\,. \tag{3}$$

As can be seen, the higher threshold voltage is independent of the supply voltage and it is determined by the reference voltage V_{ref} and the resistor ratio.

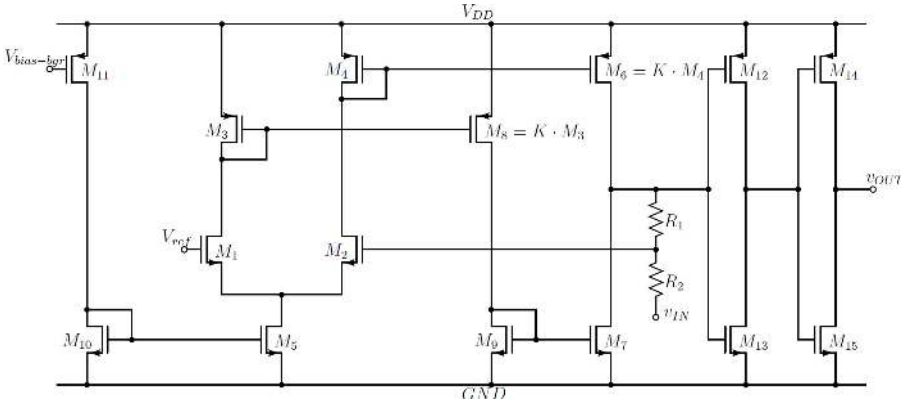

Fig. 9 – *Hysteresis comparator*.

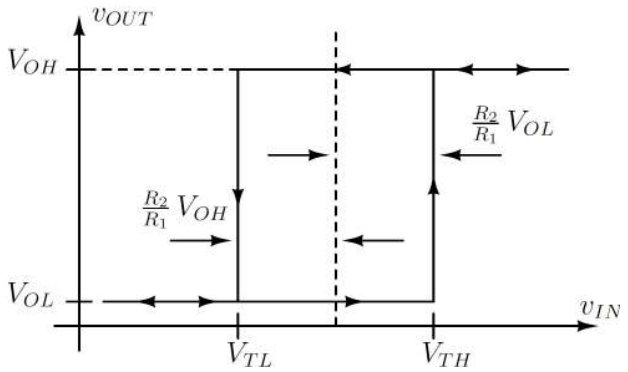

Fig. 10 – *Transfer function of the hysteresis comparator*.

The comparator senses the output voltage and forwards high voltage to COOT control if the output voltage of the Buck converter is below a desired voltage level, or low voltage if the output voltage is above the desired voltage level. Because this comparator closes the loop from Buck converter, the output voltage is given with:

$$V_{OUT} = 2V_{ref} . \tag{4}$$

Reference voltage V_{ref} is the same for the both comparators

$$V_{ref} = 600\,\text{mV} , \tag{5}$$

so the output voltage is determined to be 1.2 V. The schematic of the comparator which senses the output voltage is shown in Fig. 11. This structure has two advantages compared to Miller's amplifier. The first one, we have push-pull output stage which is suitable for the capacitive loads. The second

one, dominant pole is at the higher frequencies because we have mirrors in the first stage, thus we have higher bandwidth of the amplifier. The drawback is gain which is lower than that of Miler's amplifier and is given by:

$$A_v = g_{m1} K (r_{DS7} \parallel r_{DS6}) . \tag{6}$$

This gain is not crucial and a gain of about 50 is sufficient.

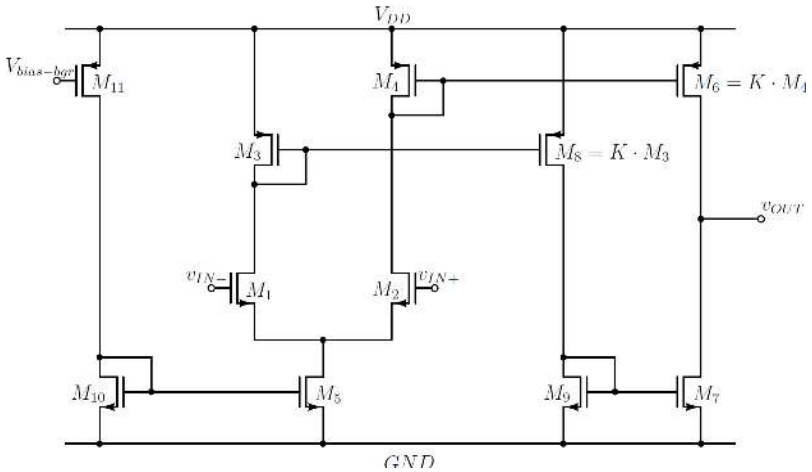

Fig. 11 – *Comparator for the output voltage sensing.*

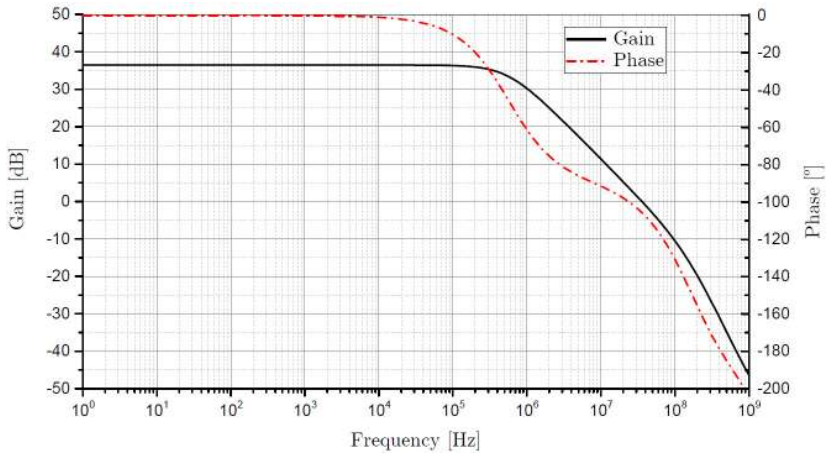

Fig. 12 – *AC response of the comparator for the output voltage sensing.*

AC response of the comparator is shown in Fig. 11. The obtained gain bandwidth of 35 MHz is an excellent result since this comparator has a very low static current consumption and a gain of about 63 (36 dB).

The voltage reference used for both comparators is shown in Fig. 13 [9].

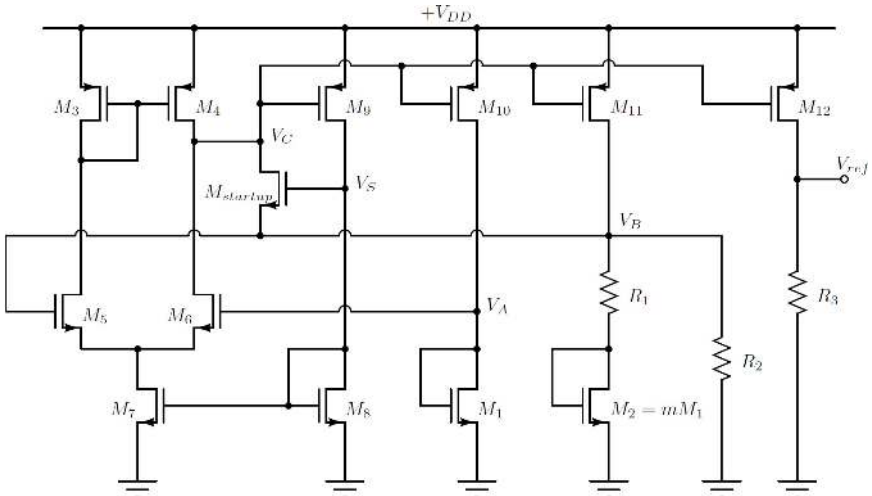

Fig. 13 – *The voltage reference.*

The voltage reference should be independent of the power supply and must have a fast transient response since the input signal is 60 GHz. The reference voltage should be stable at least for 1.5 μs if we want a correct operation of the system. Startup of the reference is obtained by only one transistor $M_{startup}$ which forms a self-biased amplifier together with transistors $M_3 - M_9$. At the beginning of the analysis, potential V_B is zero and V_S is at the high potential so the startup transistor is ON and potential V_B starts rising. When V_B has risen sufficiently, voltage between the gate and source of the startup transistor is low which turns OFF the startup transistor and the reference has stable operation. Voltages V_A and V_B have equalized, a current starts flowing through R_1 and R_2, mirrored through current mirrors $M_{10} - M_{12}$, and the reference voltage is obtained by resistor R_3. The reference voltage and current consumption are shown in Fig. 14. Transient response of the voltage reference is shown in Fig.15. The input voltage of the reference (i.e. supply voltage) starts rising and by 200ns it reaches 1.5 V. After that, the supply voltage is fixed at that value. From Fig. 15 one can see the period when the startup transistor $M_{startup}$ starts conducting (current peak of 70 μA) and the period after 1μs when the voltage reference has a stable operation.

The schematic of the whole system is shown in Fig. 16. Capacitors $C_{IN\text{-}Buck}$ and C_{OUT} are realized as MIM and MOS capacitors in parallel and they form the unit cell. In the layout, these two capacitors can be stacked one above the other because MOS capacitor is formed with respect to Metal 1 layer, while the MIM capacitors are formed between Metal 2 and Metal 5 layers.

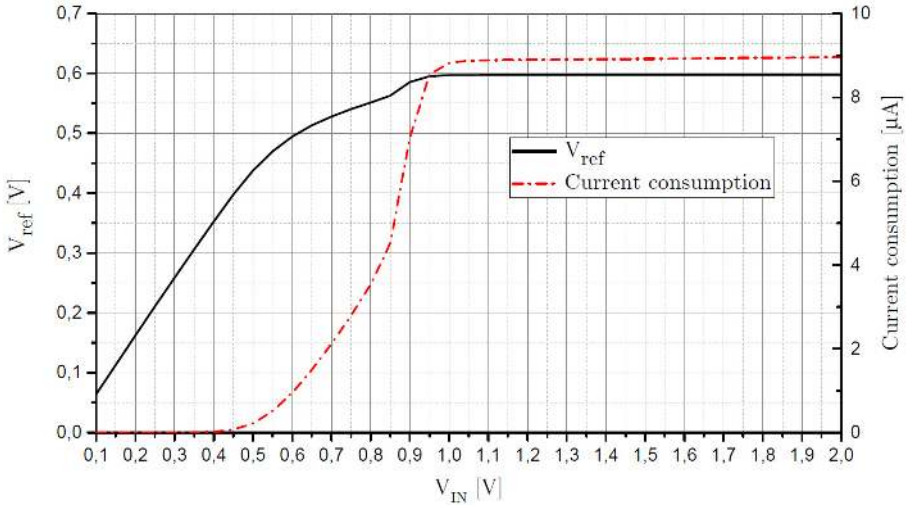

Fig. 14 – *DC response of the voltage reference.*

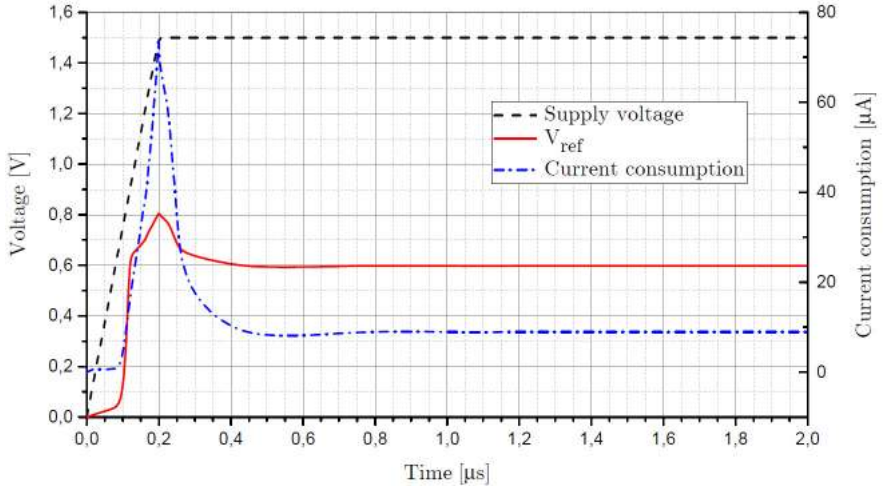

Fig. 15 – *Transient response of the voltage reference.*

With this connection the capacitance is maximized and the total area of the capacitor is minimized. The layout of the whole system is shown in Fig. 17. As mentioned earlier, capacitors $C_{\text{IN-Buck}}$ and C_{OUT} are placed around the inductors to fill the empty space in the layout. Capacitor $C_{\text{IN-Buck}}$ is located at the upper side and the upper-right side of the layout and consists of 131 parallel unit cells, while C_{OUT} is located at the lower side and lower-right side of the layout and consists of 66 parallel unit cells.

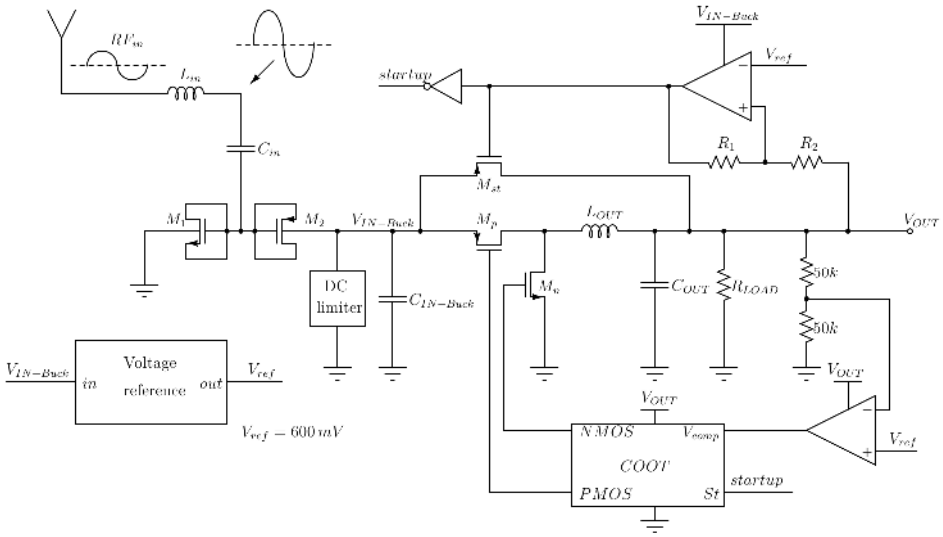

Fig. 16 – *The schematic of the whole system for RF/DC conversion.*

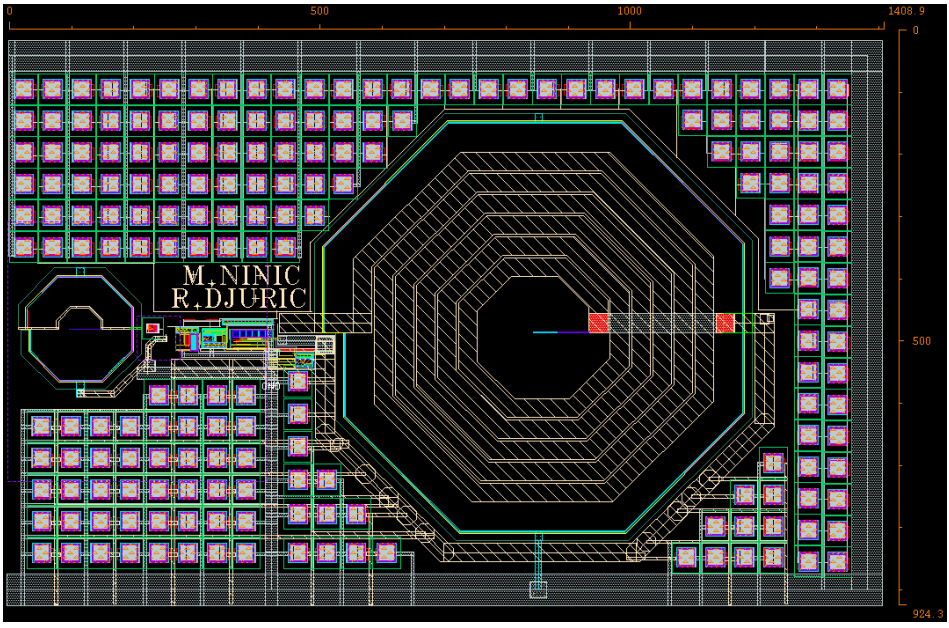

Fig. 17 – *The schematic of the whole system for RF/DC conversion.*

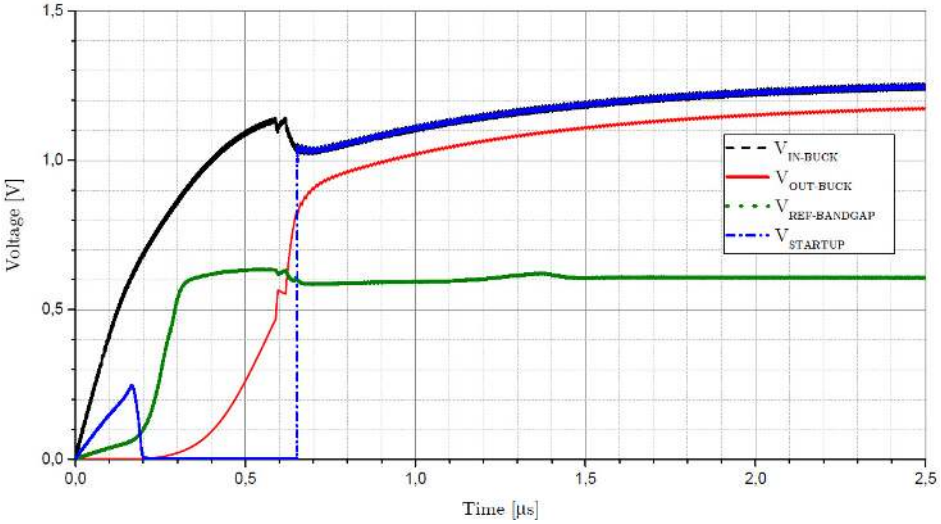

Fig. 18 – *The simulation results of the whole system.*

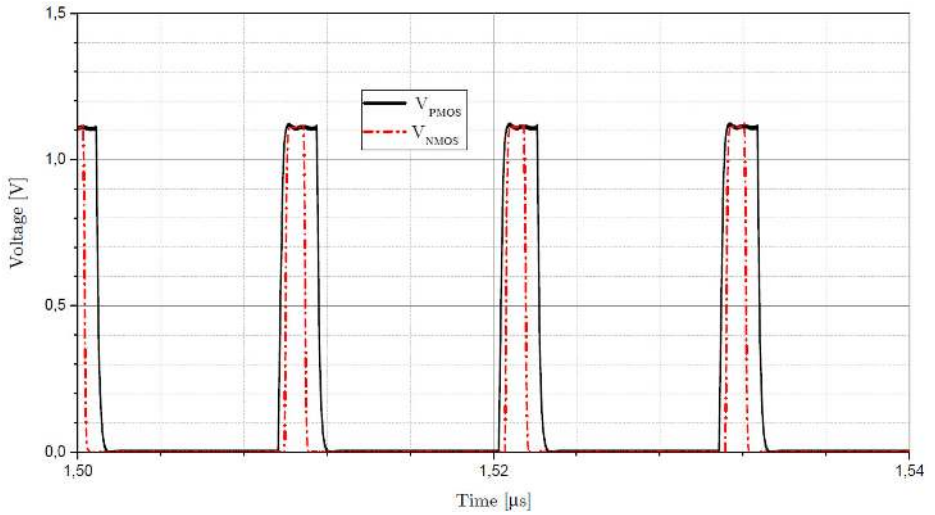

Fig. 19 – *Control signals for the PMOS and NMOS switches in the Buck converter.*

The simulation results of the whole system for a load of 1.44 kΩ are shown in Fig. 18. Several different intervals can be distinguished. The first interval, from 0 to 200 ns, is the power-up interval when the input voltage of the Buck converter (output voltage of the RF/DC converter) starts rising. After 200 ns, startup transistor M_{st} in the Buck converter is turned ON and the output voltage of the Buck converter starts rising. At 600ns output voltage of the Buck converter is about 600 mV which is enough to power-up COOT control which starts oscillating, but at a lower frequency.

Thus, the startup transistor should be turned OFF which is accomplished at 650 ns. After that, the startup transistor is turned OFF and COOT control takes over. The output voltage at the end of the simulation is about 1.2 V which results in the output power of 1 mW. The input power for this situation is

$$P_{IN} = 6.8\,\text{dBm}, \tag{7}$$

which results in the efficiency of

$$\eta = 20.89\%. \tag{8}$$

The efficiency is lowered because the Buck converter has the efficiency of about 80% for the output power of 1mW. Control signals for the PMOS and NMOS switches in the Buck converter are shown in Fig. 19. It can be seen that there is no overlapping in the switches conduction.

4 Conclusion

We have presented a novel high efficiency RF/DC power harvesting system which consist of a RF/DC rectifier and a DC/DC converter incorporating a control system for the output voltage stabilization. The rectifier has a structure of standard one-stage Dickson voltage multiplier employing diodes that have minimized parasitic capacitances. An efficiency improvement is achieved since the parasitic effect of the employed diodes is lower than the one of the standard diode connected MOSFETs. The simulation results obtained with the RC parasitic extraction showed the efficiency of 25% with 6.2 dBm input power when the rectifier is loaded by 1.44kΩ load. For this case the output voltage of the rectifier is 1.2 V, thus the output power is 1mW. In order to keep the output voltage constant, the DC/DC Buck converter is designed applying constant on/off time control system (COOT). Compared to the standard PWM control systems, COOT control system has an improved efficiency at low output powers. Since the input signal is at 60 GHz, the output voltage of the rectifier starts rising very fast and the fast transient responses of the sub-blocks are very important. The voltage reference of transient response of about 1 μs has been designed. The presented power harvesting system has the efficiency of about 21% for the output power of 1 mW.

5 References

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