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Synchronization Method for Grid Integrated Battery Storage Systems During Asymmetrical Grid Faults

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Abstract: This paper aims at presenting a robust and reliable synchronization method for battery storage systems during asymmetrical grid faults. For this purpose, a Matlab/Simulink based model for testing of the power electronic interface between the grid and the battery storage systems has been developed. The synchronization method proposed in the paper is based on the proportional-integral resonant controller with the delay signal cancellation. The validity of the synchronization method has been verified using the advanced laboratory station for the control of grid connected distributed energy sources. The proposed synchronization method has eliminated unfavourable components from the estimated grid angular frequency, leading to the more accurate and reliable tracking of the grid voltage vector positive sequence during both the normal operation and the operation during asymmetrical grid faults.

Keywords: Battery Storage Systems, Synchronization, Grid Connected Converter, Asymmetrical Grid Faults.

1 Introduction

In an effort to achieve sustainable development, the future society will need to address the key issue – increased energy demand. Future energy market will certainly include smart grid technologies, further advancing more decentralized approach to the power system. On the other hand, distributed energy generation is usually based on renewable resources with an inherited intermittency, making power flow regulation very difficult. Therefore, the development of practically applicable energy storage technologies becomes a matter of utmost importance. A possible solution can be borrowed from the automotive industry advances, where the constant increase in the number of vehicles connected to the grid is expected. The possible operation modes, grid-to-vehicle (G2V) or vehicle-to-grid (V2G), allow an electrical vehicle to present the source or the load to the

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utility grid. However, this solves the immediate issue only partially, especially for the distribution network operator (DNO), where it represents a semi-controllable intermittent and limited energy source.

A different possibility, and a more reliable one, would include distributed systems constantly accessible by the DNO. In that regard, researchers currently investigate several energy storage technologies to be used:

- Compressed Air Energy Storage – CAES,
- Thermal energy storage,
- Flywheel,
- Hydraulic and Hydro-accumulation (pump-hydro) storage,
- Electrolytic energy storage,
- Electro-chemical sources – batteries,
- Superconducting Magnetic Energy Storage – SMES, etc.

Currently, the most dominant technology for energy storage is based on electro-chemical sources, holding important advantages like the existing industry, cost-efficiency, developed technology, etc. Nevertheless, their full success has been hindered by insufficiencies such as high sensitivity, short battery life span, high price and environmental concerns [1]. Battery based storage system control needs to have high efficiency and dynamic performance, facilitating the least possible operation price. Having different algorithms impacting battery storage system output variables differently, advance methods can even aim to extend the battery lifespan (lowering the polarization effect) [2].

Constant voltage (CV) and constant current (CC) techniques present the foundation for all advanced charging methods, usually based on the hybrid CC-CV techniques [3]. The referent values and the duration, for these hybrid methods, can be calculated using some of the most advanced techniques for process optimization, including Ant Colony algorithm, Gray prediction algorithm and Particle Swarm Algorithm [4 – 6]. The control of the references is performed by different strategies and topologies like resonant controllers, hysteresis current controller, proportional-integral-derivative (PID) controller, artificial neural networks, fuzzy-logic controller and others [4, 7].

With the benefits of energy storage technologies and the subsequent increase in energy efficiency, a reliable, sustainable and economical supply can be achieved. However, the integration of the former can have adverse impact on the power quality of the system. A large number of power electronics components, introduced for the battery charging and discharging control, usually operate in a non-linear mode emphasizing this issue [8]. Therefore, advanced control strategies need to be researched, allocating special attention to the effects of battery chargers on the power quality.

Additionally, with the total integration of the battery storage system in the distribution network, the fault tolerant operation and the operation under grid faults need to be addressed. This is particularly the case for the discharging mode of the operation [9, 10], when the storage system is also required to abide by the grid code of the respective distribution network operator (DNO). In such circumstances, a reliable grid synchronization method is required in order to implement an adequate power control, restore the system stability and service the consumption, until normal grid operating conditions are restored.

This paper will attempt to present the robust method for the grid synchronization under asymmetrical grid faults. This method has no adverse influence on the system response prior to the fault occurrence, making it suitable for the full range of operations. Simulation and experimental verification of the proposed method will be presented within this paper.

2 Battery Charging and Discharging Methods

A relative unit of the energy stored in the battery, State of Charge (SOC), is used to quantify the charging process. Using SOC, one full battery cycle is defined as an alteration: SOC = 100% ⇒ SOC = 0% ⇒ SOC = 100%. When the operation mode of the battery is considered, it can be concluded that commonly either extremity is rarely reached. In such cases, the cumulative calculation of the cycle could be applied. Moreover, having separate stages for the charge and discharge process enables a fairly easy tracking of the battery cycling (it is important to note that the SOC parameter is estimated, and cannot be measured). The charge and discharge stages can be observed in Fig. 1. However, in some applications, the power flow cannot be clearly determined (overlapping of the battery operating regimes), introducing the difficulty for the identification of one full cycle (renewable resources with battery storage, regenerative braking, etc.).

With highly controllable electrical quantities, offered by the advances in modern digital control, a battery cycling can have different target values for electrical and physical quantities. The change in electrical quantities, however, is not independent of physical quantities response. This feedback can often lead to the adverse effects, especially on battery temperature. Inadequate operation of the process can also lead to a severe decrease in the battery rated capacity. More severe cases of improper control can lead to battery destruction.

Modern control techniques for grid integrated battery storage systems aim to achieve nominal values of the current (for a cycling process), keeping the presumed aging rate of the electro-chemical source. With a significant number of existing control strategies it is important to properly select the technique to be used. The optimization methods, therefore, offer various plausible possibilities [11 – 16].

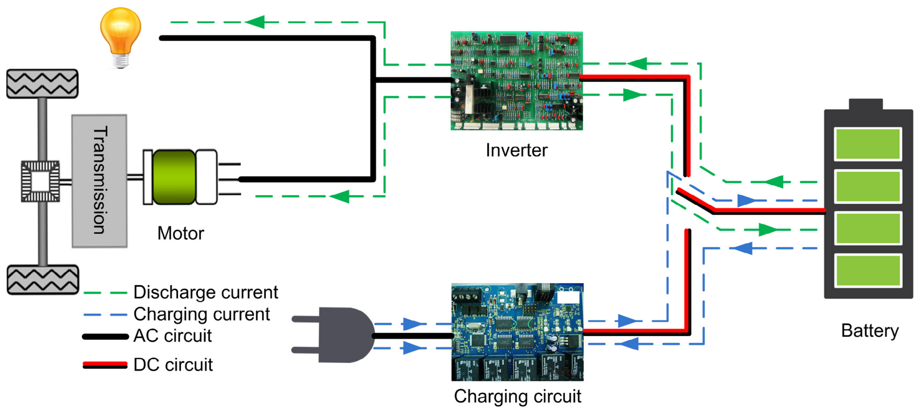

Fig. 1 – *The charging and discharging process.*

The charging process, usually classified according to the necessary time for reaching the rated capacity, can be defined by two discrete classes: fast charging and slow charging. More specifically, if the charging takes less than 1 h it is considered to be fast, while everything over 1 h is considered as slow charging (usually lasting for 10 h or more). Sometimes, the term medium charging is introduced in order to further differentiate the types of slow charging.

Another possibility for charging techniques differentiation is possible based on the controlled electrical quantity, offering techniques based on:

- current control,
- voltage control,
- current and voltage control.

The power flow control during the discharging process, even if limited by the rated values of the battery, will strongly be influenced by the requirements for the connection and operation in the distribution and transmission networks, stated in the grid code. This will force battery storage systems to behave like any other distributed generator, demanding the implementation of fault ride through (FRT) capabilities. The first step to achieving reliable FRT characteristics is to properly synchronize the battery storage system to the grid voltage vector, which can prove to be a difficult task for standard synchronization methods, especially during asymmetrical grid faults.

The selection criteria for different optimization methods and control algorithms can include the requirements for computational resources, the price of the converter components, the speed of the process, the influence on the battery aging and other physical quantities.

3 Grid Synchronization Method During Asymmetrical Faults

Modern control implies the use of digital systems, offering a relatively easy implementation of a large number of different methodologies for the grid connected converter synchronization with the grid voltage vector. The dynamic performance of the synchronization algorithm will have a significant influence on the quality of the grid connected converter control, especially for the proper power control where the precision of the grid voltage vector angle estimation will have a direct influence on the ratio of the injected active and reactive power. However, the implementation of synchronization methods is severely limited by their complexity and available processing resources. A number of different synchronization methods for the use in the grid connected converter applications are currently being proposed in the literature [17 – 20]. Many of the proposed algorithms can have a very good behaviour while the grid voltage is symmetrical, but find it difficult to correctly estimate the grid voltage angle under distorted voltages or especially under asymmetrical grid faults. In order to deal with the strict grid requirements, the existing synchronization methods have to be improved [21, 22].

3.1 Phased-Locked Loop

The synchronization methods based on the phase-locked loop (PLL) have been, since their introduction in the early 20th century, adopted in many technical fields. The technical advancement of power electronic converters, especially the grid connected converters, enabled the transfer of knowledge from other fields to the area of the grid synchronization. From there on, PLL structures have become the most commonly used mechanism for the synchronization of power electronic converters with the grid voltage vector. During that transition, the structure has been developed to answer the specific requirements in the adopting field, creating a number of different PLL based algorithms [23].

The phase locked loop uses a phase detector (PD) in order to differentiate between the phase angle of the input and the estimated angle. The acquired signal is then passed through the loop filter (LF), after which it is fed to the voltage-controlled oscillator (VCO). The estimated phase angle is generated by the VCO, and used for the control of other electrical quantities. The diagram of the PLL structure with the most common implementation is depicted in Fig. 2. It can be observed that the LF is commonly represented by the simple proportional-integral (PI) controller with the error signal integration representing the VCO. The normalized value of the estimated and the actual phase angle is used for the PD.

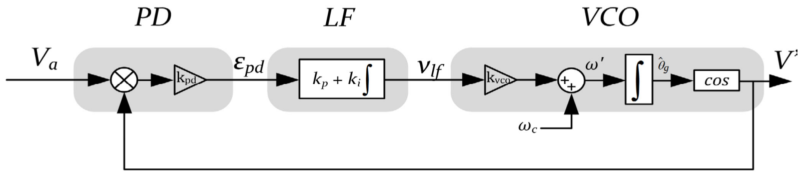

Fig. 2 – *Structure of the phase-locked loop.*

If the input and the VCO generated signals are assumed to be:

$$v = V\sin(\theta) = V\sin(\omega t + \varphi), \tag{1}$$

$$v' = \cos(\theta') = \cos(\omega' t + \varphi'), \tag{2}$$

then the error signal can be represented as follows:

$$\varepsilon_{pd} = Vk_{pd}\sin(\omega t + \varphi)\cos(\omega' t + \varphi') =$$
$$= \frac{Vk_{pd}}{2}\left[\underbrace{\sin((\omega - \omega')t + (\varphi - \varphi'))}_{\text{low frequency component}} + \underbrace{\sin((\omega + \omega')t + (\varphi + \varphi'))}_{\textit{High}\text{ frequency component}}\right]. \tag{3}$$

The high frequency component of the error signal will be negated by the loop filter (PI controller). Hence, by assuming that the VCO is tuned to the input signal frequency (i.e. $\omega \approx \omega'$) and by the linearization of the PD in the ε vicinity of the operating point (i.e. $\sin(\varphi - \varphi') \approx \sin(\theta - \theta') \approx (\theta - \theta')$), the error signal becomes:

$$\overline{\varepsilon}_{pd} = \frac{Vk_{pd}}{2}(\theta - \theta'). \tag{4}$$

With this simplified implementation, the PD is reduced to the zero order hold with the gain proportional to the signal amplitude, making the VCO frequency and the phase angle variation:

$$\overline{\omega} = (\omega_c + \Delta\overline{\omega}) = (\omega_c + k_{VCO}\overline{v}_{lf}), \tag{5}$$

$$\overline{\theta}' = \int \overline{\omega}' \,\mathrm{d}t = \int k_{VCO}\overline{v}'_{lf}\,\mathrm{d}t. \tag{6}$$

In order to integrate the PLL method into the grid connected control strategy, usually performed in the synchronous rotating (dq) reference frame, further adjustment is necessary. The synchronous frame phase-locked loop (SFPLL), provided in Fig. 3, is derived using the Park transformation. The error signal for the PI controller is acquired by subtracting the zero q-axis voltage reference from the actual q-axis voltage value, which corresponds to the alignment of the reference frame angle to the grid voltage vector d-axis component.

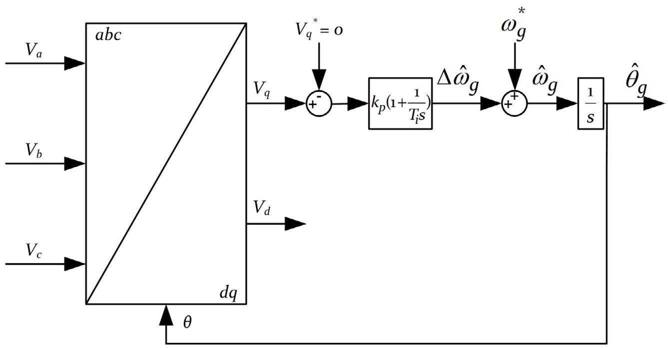

Fig. 3 – *Synchronous frame phase-locked loop.*

It is important to note that when the error signal reaches zero value the estimated angle becomes equal to the traced angle by the following rules:

$$\varepsilon = 0 - v_q = -V_g \sin\left(\theta_g - \hat{\theta}_g\right) \wedge \varepsilon = 0 \quad \Rightarrow \quad \hat{\theta}_g = \theta_g , \tag{7}$$

$$\varepsilon \approx V_g\left(\theta_g - \hat{\theta}_g\right), \tag{8}$$

$$\Delta\omega_g = G_{fil}\left(s\right)\varepsilon\left(s\right) = \left(K_p + \frac{K_i}{s}\right)\varepsilon\left(s\right) \wedge \hat{\theta}_g = \frac{1}{s}\hat{\omega}_g(s) . \tag{9}$$

The linear second order PLL transfer function in the continuous domain allows the PI controller parameters to be optimized based on the damping ratio (ξ), desired overshoot (δ), signal settling error band (*y*) and natural frequency, as follows:

$$G_{PLL}\left(s\right) = \frac{V_g K_p s + V_g K_i}{s^2 + V_g K_p s + V_g K_i} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} , \tag{10}$$

$$\xi = \frac{\left|\ln\ \delta\right|}{\sqrt{\pi^2 + (\ln\ \delta)^2}} \wedge t_{set} = -\frac{\ln\ y}{\xi\omega_n} , \tag{11}$$

$$K_i = \frac{\omega_n^2}{V_g} \wedge K_p = \frac{2\xi}{\sqrt{\frac{V_g}{K_i}}} . \tag{12}$$

3.2 Delay signal cancelation Phased-Locked Loop with the PIR controller

When asymmetrical grid faults occur, the standard SFPLL method is unable to differentiate between the positive and the negative sequence of the grid voltage, thus introducing the error in the angle estimation. The origin of the error lies within the fact that the SFPLL tracks the phase angle of the positive sequence. The negative sequence will appear as a sinusoidal component with twice the frequency of the voltage fundamental in the synchronous frame. This will cause undesired components in the estimated angle and the adverse effects on the output of the remaining controllers (power, voltage and current). In order to overcome the insufficiencies of standard the SFPLL, delay signal cancellation (DSC) before the PLL and PIR controller in the FL are introduced.

The delay signal cancellation method is commonly used for the separation of the phase-sequences in unbalanced power systems [27]. In addition, this method can be improved for this particular purpose by the introduction of the cascaded signal conditioning [28]. It is important to note that the proposed cascaded delay signal cancelation PLL introduces the delay in the control variable, and thus influences the parameters of the PLL.

In general, if we assume asymmetrical grid conditions, a voltage vector in a stationary reference frame can be represented as:

$$\underline{v}_{\alpha\beta}(t) = \underline{v}^{p}_{\alpha\beta}(t) + \underline{v}^{n}_{\alpha\beta}(t) = V^{p}\,\mathrm{e}^{\mathrm{j}(\omega_g t+\varphi_p)} + V^{n}\,\mathrm{e}^{-\mathrm{j}(\omega_g t+\varphi_p)}. \tag{13}$$

The basis of the DSC method is depicted as follows:

$$\begin{aligned} \hat{\underline{v}}^{p}_{\alpha\beta}(t) &= \frac{1}{2}\left[\underline{v}_{\alpha\beta}(t) + \mathrm{j}\underline{v}_{\alpha\beta}(t - T_g/4)\right], \\ \hat{\underline{v}}^{n}_{\alpha\beta}(t) &= \frac{1}{2}\left[\underline{v}_{\alpha\beta}(t) - \mathrm{j}\underline{v}_{\alpha\beta}(t - T_g/4)\right], \end{aligned} \tag{14}$$

with the implementation provided in Fig. 4a. When implementing the DSC method in the synchronous reference frame, further simplification is possible. The added benefit can be observed in Fig. 4b where the use of complex argument is completely avoided. For the improvement of SFPLL, the positive sequence of the synchronous reference frame is used for the grid synchronization. Negative sequence can be used to increase the precision of the angle estimation or for the adaptation mechanism in adaptive PLL structures, since the relation between the positive and the negative sequence angle is well known. The parameter T_g represents a grid voltage period, and depending on the control loop execution period, the delay is implemented by the finite number of signal sample delays.

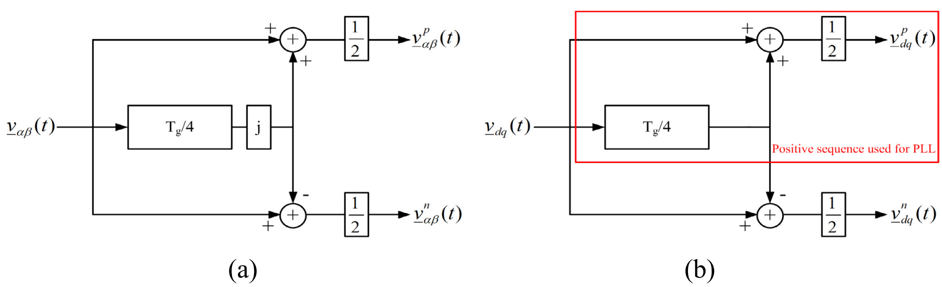

Fig. 4 – (a) *Delay signal cancellation in a stationary and a synchronous*; (b) *Reference frame.*

The usage of the standard PI controller for the loop filter has substantial benefits, such as the simplicity of implementation, the developed criteria for the parameter synthesis, and a very good dynamic performance. However, standard controllers are only able to trace constant values (hence the synchronous reference frame control). In order to be able to trace and neutralize the remaining components introduced by the voltage harmonic distortion, a new approach to the loop filter is required after DSC has been achieved. For the purpose of controlling the non-constant values, the resonant controller is added to the PI controller, creating a proportional-integral resonant controller (PIR). It will use the benefits of the standard PI controller for tracking the grid voltage angle, while allowing the resonant part to further reduce the undesired components of the error signal. The increment of the grid frequency is then found as:

$$\Delta\omega_g = G_{fil}\left(s\right)\varepsilon\left(s\right) = \left(K_p + \frac{K_i}{s} + \frac{K_i s}{s^2 + \omega^2}\right)\varepsilon\left(s\right) \wedge \hat{\theta}_g = \frac{1}{s}\hat{\omega}_g(s)\,. \tag{15}$$

For this improved synchronization method the parameters for the PI part of the controller will remain the same. While the resonant part of the controller uses the same integral gain, it is tuned to different frequency components. Additionally, it is even possible to implement multiple resonant elements in order to reduce different signal components (from different harmonic orders).

4 Simulation Model and Results

In order to investigate the PLL technique behaviour during grid faults, the simulation model of the grid connected converter in Matlab/Simulink has been developed. The model is completely adapted to correspond to the actual laboratory prototype available for testing the behaviour of grid integrated distributed energy sources [29]. The switching model of the converter is used, the grid is modelled by the Thevenin's equivalent circuit and the control algorithm is modified to mimic the actual task oriented digital controller implementation [30]. Current control is located in the 4 kHz sampling frequency task and measurement in the 8 kHz sampling frequency task.

From the frequency response of the classical PLL loop filter (PI controller), provided in Fig. 5, the stability of the system can be observed. Frequency response is generated using the loop filter transfer function presented in Eq. 9. It can be noted that the chosen PI controller parameters will always lead the classical PLL to a stable steady-state response. However, this classical approach could have some undesired effects, since the gain response shows a significant amplification of the higher low order harmonic sequences of the signal, which in turn leads to the necessity of the controller parameter correction. In that regard, it is necessary to reduce those components prior to the synchronization.

If we assume the same integral gain as for the PI controller, the PIR filter transfer function depicted in (15) will have the frequency response shown in Fig. 6. The introduction of the resonant structure in the controller will allow for the easier mitigation of undesired components, by simple tuning of the PIR controller resonant frequency. In this particular case, the resonant frequency is set at the second order harmonic sequence of the grid voltage vector.

In order to demonstrate the benefits offered by introducing the DSC algorithm and the PIR controller to the PLL loop, two parallel PLL structures are excited by the same three-phase system of voltages. At one point, the grid switches from symmetrical voltages to the asymmetrical voltage dip. This usually occurs during the most common grid faults, like one- and two-phase short circuits. In order to compensate for the voltage and power unbalance, the grid connected converter will need to stay active, and supply the grid during the faults, which in turn means operating under sometimes severe asymmetry. Therefore, the synchronization unit has to successfully track the positive voltage sequence of the grid, and negate the influence of the negative sequence.

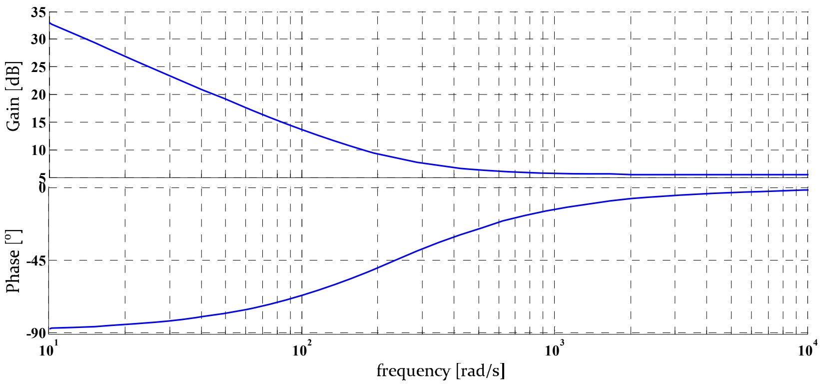

Fig. 5 – *Graph of the classical PI frequency response.*

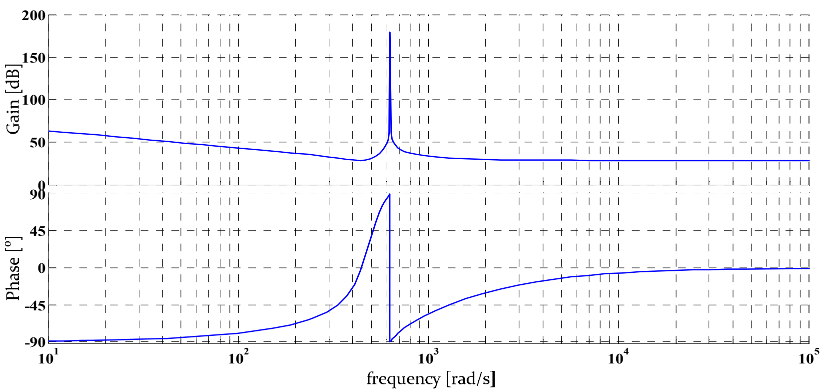

Fig. 6 – *Graph of the PIR frequency response.*

The correct estimation of the grid voltage phase angle is only possible with the precisely estimated grid frequency, as the input to the VCO segment. If the estimated grid frequency contains undesired harmonic values, this will be replicated in the estimated phase angle, and thus forwarded to the terminal values such as power and current. In order to test the behaviour of the classical and the improved PLL, symmetrical positive sequence grid voltages have been applied to the system from the beginning. At 0.4 s the system is switched to the two-phase 30 % voltage dip, as observed in Fig. 7. The response of the PLL unit for the estimated grid angular frequency is presented in Fig. 8. It can easily be concluded that, in the presence of grid faults, the classical PLL structure contains unfavourable components twice the frequency of the fundamental. The response for both synchronization methods is clearly stable leading the remaining control system in the steady state.

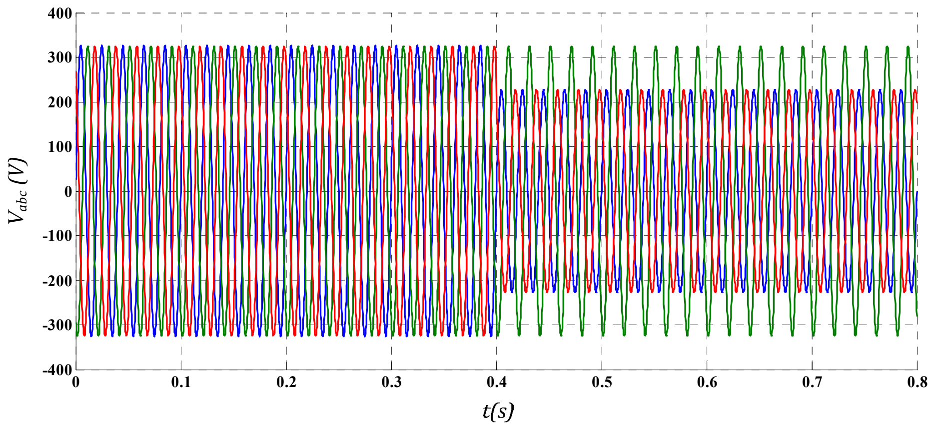

Fig. 7 – *Grid voltages applied to the grid connected converter.*

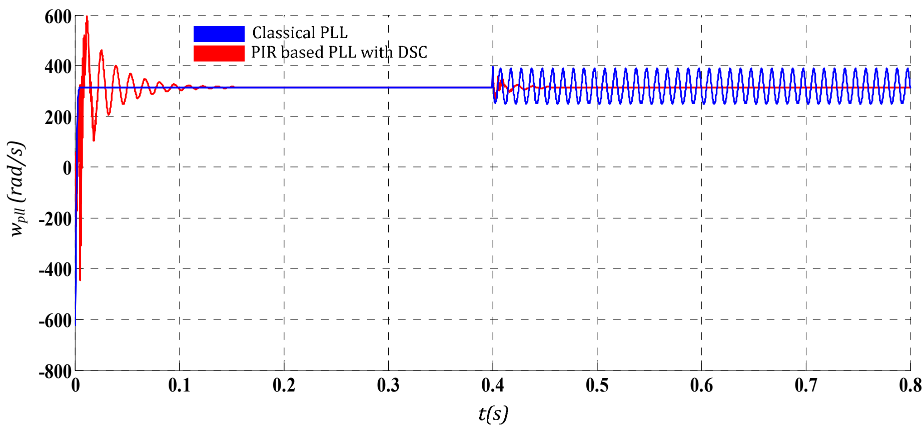

Fig. 8 – *Grid angular frequency estimation.*

However, the classical PLL shows a repetitive error in the angular frequency, and therefore in the phase angle estimation, making it unreliable during grid faults. The PIR based PLL with DSC has a more beneficial response during asymmetrical grid conditions, where the undesired components are completely mitigated. Additionally, both PLL structures have achieved the same steady state response under symmetrical conditions. It could be argued, and rightfully so, that the settling time of the improved PLL method is somewhat longer than the one for the classical counterpart. Although slower, the precision of the new algorithm is far more beneficial, and furthermore the response of the improved method to the disturbance is significantly faster than to the excitation.

The error introduced by the classical PLL can clearly be observed through the estimated angle value illustrated in Fig. 9.

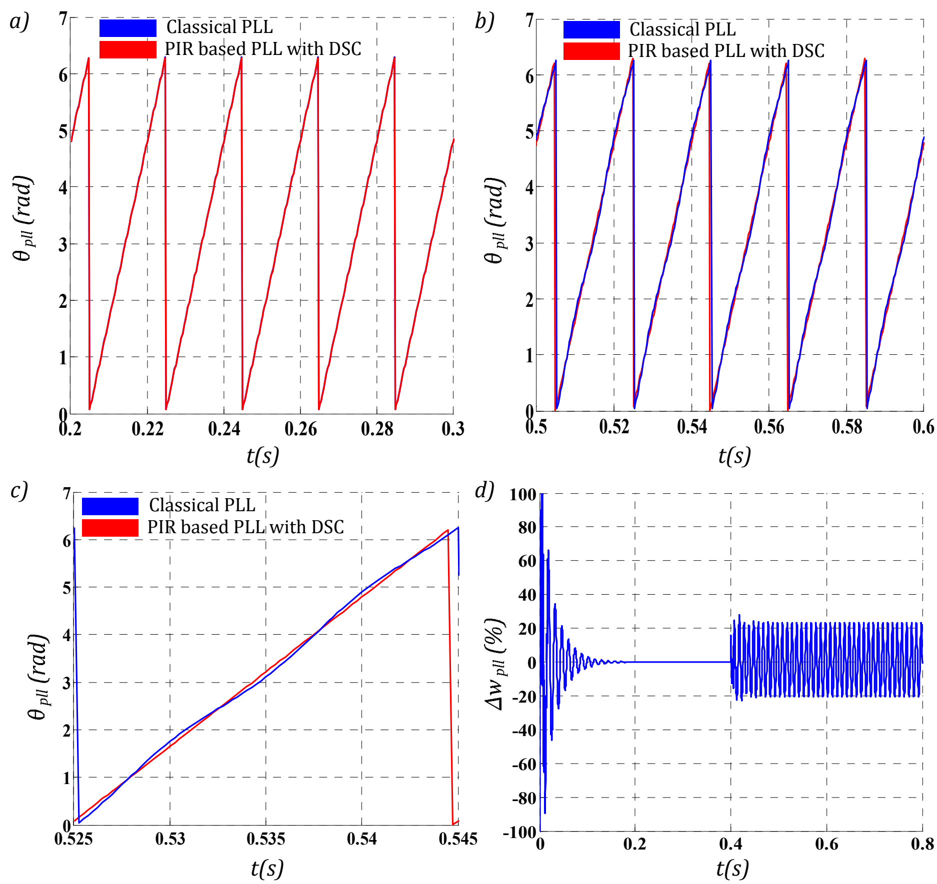

Fig. 9 – *Estimated value of the grid angle for the symmetrical (a) and the asymmetrical (b) grid conditions with the single grid period (c) and the estimation error (d) of the classical PLL in regard to the PIR based PLL with DSC.*

Both the classical and the PIR based PLL have had no problems while tracking the grid angle for a positive sequence symmetrical grid voltages, clearly having the same responses as noted in Fig. 9a. After the grid conditions have changed, a clear difference in the angle estimation can be noted (Fig. 9b), while the oscillation in the estimated angular frequency for the classical PLL can be observed in the estimated angle as well (Fig. 9c). This subsequently leads to the increase of negative sequence current components, through an inadequate position of the synchronous reference frame used for the current control. The repetitive error of the classical PLL relative to the PIR based PLL can be observed in Fig. 9d, where it reaches the inadmissible 20 %.

5 Experimental Verification

The behaviour of the synchronization unit for the grid connected converter was tested on an advanced laboratory prototype, developed at the Faculty of Technical Sciences [29, 30]. The laboratory setup comprises of the state-of-the-art hardware in the field of electrical drives and control. The base of the setup is the highly modular dSPACE control hardware [31]. The outlook of the overall system can be observed in Fig. 10. This system is paired with the grid emulator GE15 that has the capability for providing adjustable grid voltages for testing the system under different conditions (i.e. grid fault) [32]. Using the grid emulator close to ideal sinusoidal voltages, with THD less than 0.5%, were set at the point of common coupling (PCC). In that regard, the influence of the distorted grid can almost completely be disregarded. At a certain point, the grid emulator was set to generate 20 % voltage dip in two-phases in order to behave as a grid under the asymmetrical fault. After observing the PLL unit responses, the voltage was restored to symmetrical conditions. The voltage waveforms at the PCC are depicted in Fig. 11.

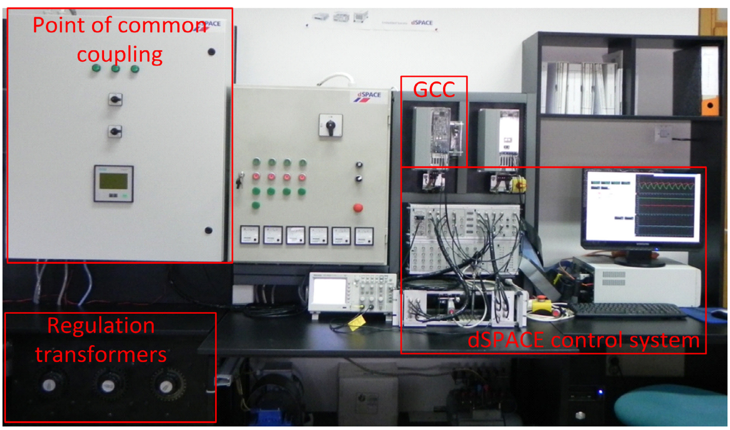

Fig. 10 – *Advanced laboratory setup for testing the grid connected distributed energy resources.*

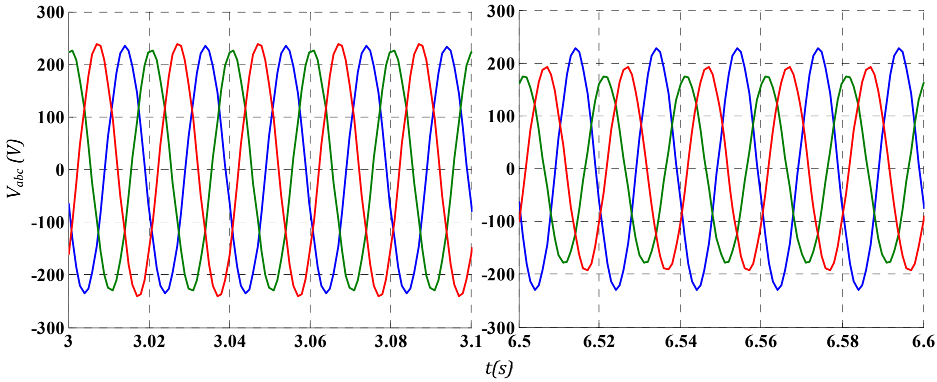

Fig. 11 – *Emulated grid voltage waveforms.*

For this experiment, the voltage dip was emulated for 6 seconds after the experiment had started, and the voltage was restored between 10th and 11th second. It is important to note that the experiment, unlike the simulation, began when the symmetrical voltages were present. In Fig. 12, the grid angular frequency estimation response is provided for the complete duration of the experiment. The inability of the classical PLL to cope with the negative sequence components is clearly exhibited, making the complete control system for the grid connected converter unreliable. The classical PLL structure angular frequency response oscillates between 303 rad/s and 325 rad/s for 50 Hz grid frequency, during the asymmetrical grid voltages. The improved PLL structure response remains constant throughout the experiment, adequately tracing the grid angular frequency at 314 rad/s. The oscillations in the experiment were somewhat lower than for the simulation, due to the sampling and processing of the measured voltage signal prior to the synchronization unit.

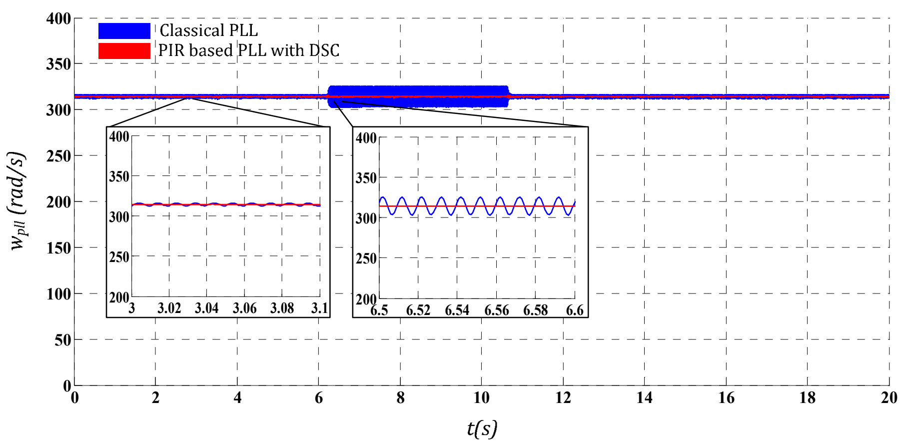

Fig. 12 – *Experimental verification of grid angular frequency estimation.*

Further verification of the simulation results and theoretically proposed explanations can be seen in Fig. 13. The unfavourable effects of the classical PLL during the grid faults are transferred to the angle estimation, as can be observed in Fig. 13a and 13b. The high percentage matching of the signal is achieved for the symmetrical steady state, while the difference is clearly present during asymmetry. The error made by the classical PLL relative to the PIR based PLL with DSC can be observed in Fig. 13c. In contrast to the simulation, the error also exists in the symmetrical steady state response, with the amplitude of around 0.5 %. This is not a significant error, and its presence can be explained by the slight harmonic distortion of the applied voltage, where the improved PLL also manages to mitigate these side effects. For the asymmetrical operating regime, the error is in accordance with the proposed theoretical aspects and simulation results. Experimental verification proves the benefits offered by the improved PLL technique based on the PIR controller with the implemented DSC.

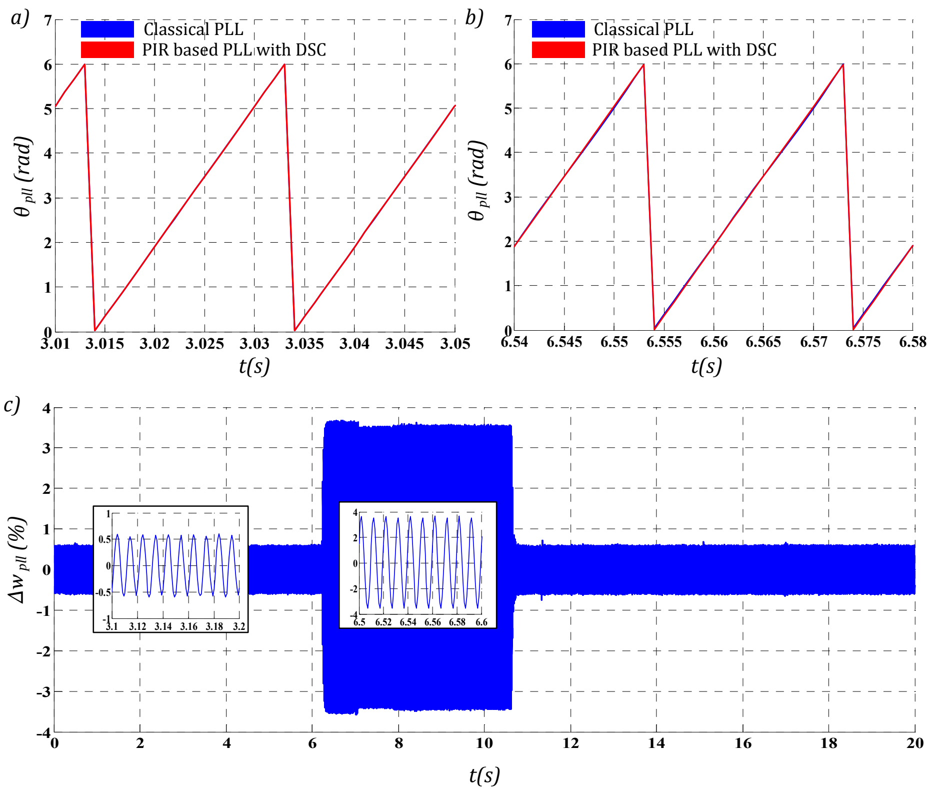

Fig. 13 – *Estimated value of the grid angle for symmetrical (a) and asymmetrical (b) grid conditions and the estimation error (c) of the classical PLL in regard to the PIR based PLL with DSC.*

During the rated operating conditions, both the classical PLL, proposed in [17] and [23], and the proposed technique have the same behaviour. However, the main benefit of the PIR based PLL with DSC is the ability to provide the reliable synchronization even when asymmetrical grid faults occur. For asymmetrical voltages, synchronization techniques are usually based on filtering and averaging the grid voltages, like in [33 – 35]. Another possibility, as explained in [23], is to use the improved PLL methods such as Double synchronous frame PLL (DSF-PLL), Double second order generalized integrator PLL (DSOGI-PLL), Three-phase magnitude PLL (3MPLL), etc. The delay introduced by the PIR based PLL with DSC is significantly lower than for the most filtering and averaging based methods, since the DSC is performed in the synchronous reference frame and tuned to the second order harmonic component corresponding to the inverse grid voltage sequence. In addition, unlike most filtering and averaging methods, as well as some improved PLL methods like DSF-PLL, the proposed method is able to completely negate the undesired components due to the introduction of the resonant controller. Different from most other techniques, the added benefit of the proposed technique is the simplicity of implementation, requiring almost no additional computational resources in regard to the classical PLL.

6 Conclusion

In order to achieve sustainable development in the future, energy market and especially electrical energy market has to follow new trends by the continuous integration of new and advanced technologies. Without any doubt, decentralized units for energy storage, especially grid connected battery storage systems, will be placed in the heart of future and emerging technologies. In that regard, the grid connected converter will take a pivotal role in the future of energy trading, and with that, the rules and requirements for the interconnection between the grid and the converter will become stricter. Currently, the corner stone of every grid code is providing the fault ride through capabilities for every distributed energy resource. Even if severely limited by their capacity, especially during the discharge process, battery storage systems connected to the grid will have to abide by the same principles as other distributed energy resources. Consequently, in the set of important requirements, the first issue will be the safe, reliable and precise synchronization to the grid voltage vector, especially during grid faults.

Several methods for synchronization have been proposed in the literature, yet in order to achieve satisfactory dynamics, experts have always turned to the phase-locked loop algorithm. Nevertheless, these algorithms sometimes have adverse responses when applied to asymmetrical grid voltage conditions or during other disturbances. This can particularly cause a problem for grid current and power controllers, causing them to introduce unfavourable components to the injected values at the point of common coupling.

In order to overcome these insufficiencies, this paper proposes the use of the improved PLL based on the PIR controller for the loop filter and with the delay signal cancellation implemented in the stationary reference frame. As presented, when grid voltages are transformed to the synchronous reference frame, it is necessary to differentiate between the positive (constant) and negative (oscillatory) component of the voltage vector in order to correctly track the positive sequence voltage angle. Sequence separation is performed using DSC, and the remaining oscillatory components are mitigated by appropriate tuning of the resonant controller segment. The PIR based PLL with DSC is capable of successfully tracking the grid voltage vector position during both operating regimes, while making a significant improvement at the angle estimation during asymmetrical grid faults.

The benefits of the improved PLL shown through the simulation were experimentally verified using an advanced research and a development station for the control of the grid connected distributed energy sources.

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