SERBIAN JOURNAL OF ELECTRICAL ENGINEERING
Vol. 11, No. 2, June 2014, 269-290

UDC: 621.382.3:621.391.814 **DOI: 10.2298/SJEE140106022D**

Analytic Models of CMOS Logic in Various Regimes

Branko Dokić[1], Tatjana Pešić-Brđanin[1], Radoš Dabić[1]

Abstract: In this paper, comparative analytic models of static and dynamic characteristics of CMOS digital circuits in strong, weak and mixed inversion regime have been described. Term mixed inversion is defined for the first time. The paper shows that there is an analogy in behavior and functional dependencies of parameters in all three CMOS regimes. Comparative characteristics of power consumption and speed in static regimes are given. Dependency of threshold voltage and logic delay time on temperature has been analyzed. Dynamic model with constant current is proposed. It is shown that digital circuits with dynamic threshold voltage of MOS transistor (DT-CMOS) have better logic delay characteristics. The analysis is based on simplified current-voltage MOS transistor models in strong and weak inversion regimes, as well as PSPICE software using 180 nm technology parameters.

Keywords: CMOS digital circuits, Weak inversion, Strong inversion.

1 Introduction

During the last two decades, researchers and manufacturers have focused on the circuits with very low power consumption [1, 2]. At first, development has been carried out in two directions: technological and logical [3, 4]. The former was towards lowering standard CMOS digital logic transistor dimensions in the scaling process [5, 6] and decreasing power supply voltage, hence reducing power consumption. The latter was oriented towards alternative topologies of digital logic, such as: differential and pass logic [7], complementary pass logic, push-pull pass logic [8] and multi-level CMOS digital logic [9]. A special group consists of dynamic CMOS circuits [10, 11] and various topologies of CMOS adiabatic logic [12, 13].

In the last ten years, focus was on sub-threshold CMOS logic [14 – 17]. Power supply voltage V_{dd} has been lower than the MOS transistor threshold voltage V_t ($V_{dd} < V_t$). Transistor operating currents, in weak inversion regime, are several orders of magnitude lower than in strong inversion regime. Therefore, operating speed of sub-threshold logic is lower for the same order of magnitude. However, electronic systems such as wireless sensor nodes and

[1]Branko Dokić, Faculty of Electrical Engineering, University of Banja Luka, Patre 5, 78000 Banja Luka, Bosnia and Herzegovina; E-mails: bdokic@etfbl.net, tatjanapb@etfbl.net, rados.dabic@etfbl.net

medical devices operate at relatively low frequencies completely covered by sub-threshold logic. Since the power supply voltages are only several hundreds of millivolts, electrical energy consumption is very low (about picowatt). Thanks to that fact, sub-threshold logic is nowadays unrivalated in digital systems with autonomous power supply [18, 19].

Until a decade ago, weak inversion regime was primarily used in MOS and CMOS analog circuits. Today, both MOS transistor regimes, weak and strong inversion, are equally exploited in digital circuits as well. There are slight differences regarding consumption and speed, which determines digital logic fields of application in these two regimes.

Although the analytic models of MOS transistor current-voltage characteristics in weak and strong inversion regimes are very different, there is a complete analogy between operation and parameters of CMOS digital logic in them [20], and that will be shown in this paper. Regarding to that fact, CMOS digital system design techniques using transistors in weak and strong inversion regimes are pretty much the same. It significantly reduced time of sub-threshold logic appliance in commercial digital devices.

As previously known, there are three MOS transistor operating regimes [21]: weak, moderate and strong inversion. Usually, CMOS logic is divided in two regimes: sub-threshold (weak inversion) and over-threshold (strong inversion). However, this paper also indicates the third, mixed operating regime of CMOS digital logic. In the area of power supply voltage $V_t < V_{dd} < 2V_t$, where $V_t = V_{tn} = |V_{tp}|$ represents nMOS or pMOS transistor threshold voltage, CMOS inverter transistors operate in both weak and strong regimes in the transition area. For that reason, it is proposed that this operating regime is called mixed inversion. It will be shown that static parameters of the mixed regime are equal to the ones in sub-threshold regime, and dynamic parameters are equal to those in strong inversion regime.

2 Three Regimes of MOS Transistor

There are three regimes of MOS transistor static characteristics [21]. Mathematical model for all three regimes is given by:

$$I_{ds} = \frac{W}{L}\mu C'_{ox}(2n)\phi_t^2 \left\{ \left[\ln\left(1+e^{\frac{V_{gs}-V_t}{2n\phi_t}}\right) \right]^2 - \left[\ln\left(1+e^{\frac{V_{gs}-V_t-nV_{ds}}{2n\phi_t}}\right) \right]^2 \right\}. \quad (1)$$

This equation is very complex and impractical for non-machine analysis. On the other hand, moderate inversion is usually disregarded and in literature treated as a peak of weak, or mostly as a bottom of strong inversion [22]. Therefore, it is

usually considered that for $V_{gs} > V_t$, transistor operates in strong inversion regime, and for $V_{gs} < V_t$ in sub-threshold regime (weak inversion). From the point of view of today's applications, it can be said that V_t stands for gate-source voltage at the boundary of strong and weak inversion.

It is well known that $I_d(V_{ds}, V_{gs})$ characteristics in strong inversion regime have two regions, saturated and non-saturated (2):

$$I_d = \begin{cases} k\left[2\left(V_{gs} - V_t\right)V_{ds} - V_{ds}^2\right], & V_{ds} < V_{gs} - V_t \\ k\left(V_{gs} - V_t\right)^2, & V_{ds} > V_{gs} - V_t \end{cases} \tag{2}$$

where:

$$k = \frac{\mu C_{ox}}{2t_{ox}}\left(\frac{W}{L}\right).$$

In non-saturated region, $V_{ds} < V_{gs} - V_t$, drain current is square function of drain-source voltage (V_{ds}) and linear function of gate-source voltage (V_{gs}). In saturated region, drain current is $I_d \sim V_{gs}^2$ and does not depend on of V_{ds}, i.e. $I_d \sim const$ is a function of V_{ds}.

MOS transistor characteristics in weak inversion regime are defined by:

$$I_{Dsub} = \begin{cases} I_0 \, \mathrm{e}^{\frac{V_{gs} - V_t}{n\phi_t}} \left(1 - \mathrm{e}^{-V_{ds}/\phi_t}\right), & V_{ds} < 3\phi_t \\ I_0 \, \mathrm{e}^{\frac{V_{gs} - V_t}{n\phi_t}}, & V_{ds} > 3\phi_t \end{cases} \tag{3}$$

where:

$$I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)\phi_t^2 \tag{4}$$

represents drain current at the boundary of weak and strong inversion regime. Parameters given in (1) and (4) have meanings as follows: μ_0 is a mobility of major charge carriers (electrons and holes in nMOS to pMOS transistor), $C_{ox} = \varepsilon_{ox} / t_{ox}$ is gate capacitance (ε_{ox} is a dielectric constant, t_{ox} is a thickness of the gate oxide), W and L are width and length of the channel, respectively, $\phi_t = kT/q$ is a thermal potential ($\phi_t = 26\,\mathrm{mV}$ at $T = 300\,\mathrm{K}$), $n = 1 + C_d / C_{ox} \approx 1.5$ is a gradient factor. For $V_{ds} > 3\phi_t$, drain current almost does not depend on the voltage V_{ds} [19], so that the region, analogous to strong inversion regime, can be treated as saturated region. In this region it holds $I_d \sim e^{V_{gs}}$. For $V_{ds} < 3\phi_t$,

at $V_{gs} = \text{const.}$ $I_d \sim e^{V_{ds}}$, transistor is in non-saturated region. In both weak and strong inversion regimes, $I_d(V_{ds}, V_{gs})$ characteristics have saturated and non-saturated region, provided that in the strong inversion regime boundary between those regions depends linearly on the V_{gs} ($V_{gs} = V_{ds} - V_t$). In weak inversion regime, that boundary is fixed ($V_{ds} = 3\phi_t$) and independent on V_{gs} voltage.

3 Three Regimes of CMOS Logic

As previously mentioned, threshold voltage is gate-source voltage boundary between strong and weak inversion of MOS transistor. Therefore, it is wrongly considered that CMOS logic can operate in just two regimes – weak and strong inversion. As it will be shown on the CMOS inverter example (Fig. 1), there is a third regime called mixed regime.

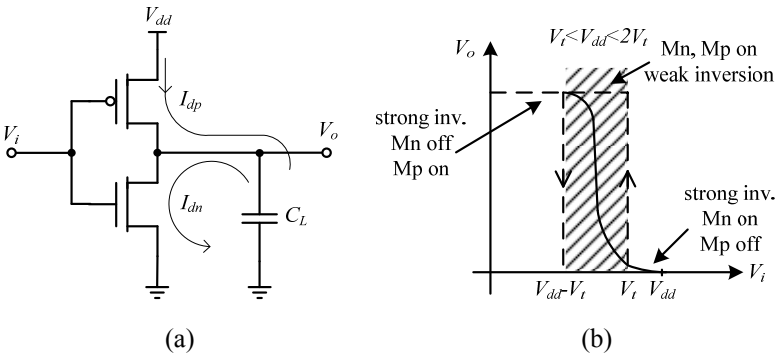


Fig. 1 – *CMOS inverter (a) strong and weak inversion area on transfer characteristic in mixed regime (b).*

Supply voltage areas of the CMOS logic operating regimes are shown in **Table 1**. For the weak inversion is:

$$3\phi_t < V_{ddsub} < V_t = V_{tn} = |V_{tp}|. \tag{4}$$

Both nMOS and pMOS transistors, while $V_{dd} < V_t$, operate in weak inversion regime for complete range of input voltage $0 \le V_t \le V_{dd}$. Lower limit should be $V_{dd\,\min} = 3\phi_t = 78\,\text{mV}$ (for $T = 300\,\text{K}, V_{dd} < V_t$), because that is the limit between saturated and non-saturated area where satisfying quality of transfer characteristic $V_o - V_i$ still exists (sufficiently narrow transition area). Some authors determine minimum supply voltage using by criterion that logic circuits are able to distinguish two discreet states. For example, authors in [14] state the limitation $V_{dd} > 57\,\text{mV}$, and authors in [23] $V_{dd} > 48\,\text{mV}$.

Table 1
Operating voltage range for three CMOS regimes.

	Inversion		
	Weak	Strong	Mixed
Power supply	$3\phi_t < V_{dd} < V_t$	$V_{dd} > 2V_t$	$V_t < V_{dd} < 2V_t$

As a strong inversion in logic circuit should be considered operating regime in which there is a part of transfer characteristic where both nMOS and pMOS transistors are conductive ($V_{gsn} > V_{tn}$ and $|V_{gsp}| > |V_{tp}|$), i.e. in strong inversion regime. This will apply if $V_{gsp} = V_{tn} - V_{dd} < V_{tp}$, from where the requirement for strong inversion of CMOS logic is as follows:

$$V_{dd} > V_{tn} + |V_{tp}| = 2V_t. \tag{6}$$

In the range

$$V_t < V_{ddm} < 2V_t \tag{7}$$

there is no area of transfer characteristic where both nMOS and pMOS transistors operate in strong inversion regime (Fig. 1b). Conversely, in the transfer characteristic area where $V_{ddm} + V_{tp} < V_i < V_{tn}$, both nMOS and pMOS transistors are in sub-threshold regime. For $0 \le V_i \le V_{ddm} + V_{tp}$ pMOS transistor is conductive, and for $V_{tn} \le V_i \le V_{ddm}$ nMOS transistor is conductive, which corresponds to CMOS strong inversion regime. In other words, when condition (7) is fulfilled, either nMOS ($V_{gsn} > V_{tn}$) or pMOS ($|V_{gsp}| > |V_{tp}|$) transistor is conductive, which corresponds to CMOS strong inversion regime. In the transition area, where logic state changes, both transistors are in sub-threshold regime which applies to weak inversion regime. Therefore, mixed inversion term is proposed.

4 Static Models in CMOS Weak and Strong Inversion Regimes

From the analogy of MOS transistor characteristics in weak and strong inversion regimes, corresponding analogy of analysis and logic circuit characteristics is carried out in various CMOS regimes. It has to be added that appropriate topologies are the same for all regimes. It is assumed that the reader is familiar with logic circuit characteristics in CMOS strong inversion regime. Consequently, analytic models of basic parameters in CMOS weak inversion regime and their comparison to strong inversion regime are given here.

4.1 Static transfer characteristics

Figure 2 presents voltage and current (dashed line) transfer characteristics of inverter in weak inversion regime, using PSPICE analysis. It is evident that the characteristics shape is completely the same as in CMOS strong inversion regime. Functional dependencies in transition area are different, of course. For example, current from power source I_{dd} in strong inversion regime is quadratic, while I_{ddsub} in weak inversion regime is exponential function of input voltage. I_{dd} has been defined with (2), and I_{ddsub} with (3) in saturated area, or:

$$I_{ddsub} = \begin{cases} I_{on}\, \mathrm{e}^{\frac{V_i - V_T}{n\phi_t}}, & 0 < V_i - V_{Tsub}, \\ I_{op}\, \mathrm{e}^{\frac{-V_i + V_{dd} - V_T}{n\phi_t}}, & V_{Tsub} < V_i < V_{ddsub}. \end{cases} \tag{8}$$

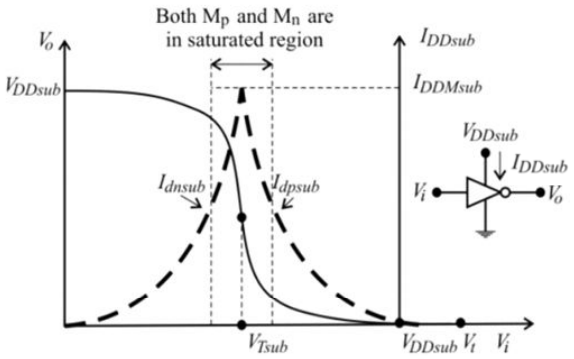


Fig. 2 – *Inverter characteristics* $V_o - V_i$ *(solid line) and* $I_{ddsub} - V_i$ *(dashed line) in CMOS sub-threshold regime.*

In both regimes, inverter threshold voltage V_T is located in part of $V_o - V_i$ characteristic where both transistors are in saturated region. Considering that $V_{gsn} = V_i$ and $V_{gsp} = V_i - V_{dd}$, equalizing nMOS and pMOS transistors currents in saturated area and replacing $V_i = V_T$ from (2) gives:

$$V_T = V_{Tn} + \frac{V_{dd} + V_{tp} - V_{tn}}{1 + \sqrt{\dfrac{\mu_n W_n / L_n}{\mu_p W_p / L_p}}} \tag{9}$$

for strong inversion, and from (3):

$$V_{Tsub} = \frac{V_{ddsub}}{2} - \frac{n\phi_t}{2} \ln \frac{I_{on}}{I_{op}} \tag{10}$$

for weak inversion regime. If the inverter is symetric, i.e. for:

$$\frac{k_n}{k_p} = \frac{I_{on}}{I_{op}} = \frac{\mu_n W_n / L_n}{\mu_p W_p / L_p} \tag{11}$$

then threshold voltage in both regimes is equal to the half of the supply voltage ($V_T = V_{dd}/2$ and $V_{Tsub} = V_{ddsub}/2$). Transfer characteristics in both regimes, besides from supply voltage, are dependent on CMOS transistors geometry ratio (Fig. 3).

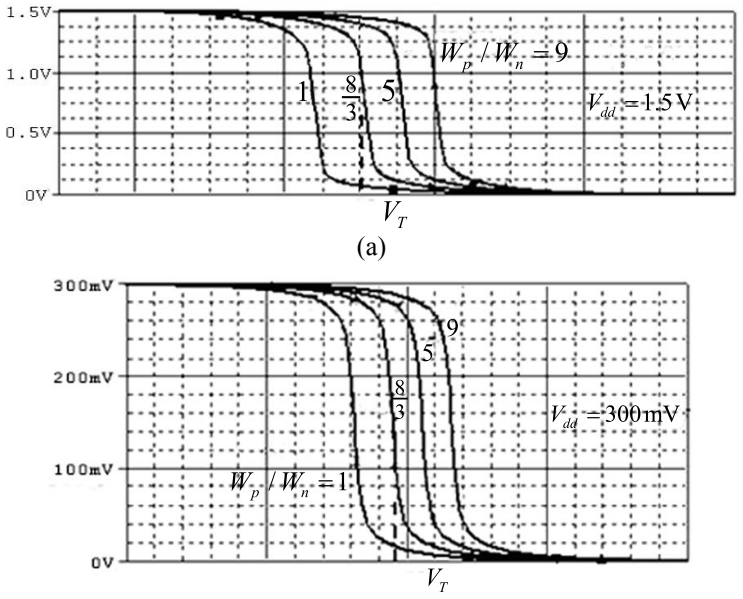


Fig. 3 – *$V_o - V_i$ inverter transfer characteristics in (a) strong and (b) weak inversion regime for different W_p / W_n ratio.*

Maximal short circuit current is obtained at $V_i = V_T$, so that according to (2) in saturated area and (3):

$$I_{ddM} = \mu_n \frac{C_{ox} W}{2L} \frac{\left(V_{dd} - 2V_t\right)^2}{\left(1 + \sqrt{\frac{\mu_n W_n / L_n}{\mu_p W_p / L_p}}\right)^2} \tag{12}$$

in strong inversion regime, and based on (8) and (10):

$$I_{ddMsub} = I_{on} \sqrt{\frac{I_{op}}{I_{on}}}\, \mathrm{e}^{\frac{V_{ddsub}/2 - V_t}{n\phi_t}} \tag{13}$$

in weak inversion regime. For $V_t = 500\,\text{mV}$, $V_{dd} = 1.5\,\text{V}$, and $V_{ddsub} = 350\,\text{mV}$, this current ratio for symetric inverter is $I_{ddM} / I_{DDMsub} = 0.22 \cdot 10^6$. So, short circuit current maximum in weak inversion regime is lower about five orders of magnitude than in strong inversion regime.

4.2 Power consumption

Analytic expressions for static power consumption:

$$P_S = V_{dd}\left(I_{dss} + I_{dsub} + I_g\right) \tag{14}$$

as well as for dynamic consumption of electrical energy:

$$P_d = C_L V_{dd}^2 f \tag{15}$$

are equal for both weak and strong inversion.

In (14), I_{dss} represents the current of inverse polarized p-n junction drain-source, and $I_{dsub} = I_0 e^{-V_t / n\phi_t}$ is sub-threshold current while $V_{gs} = 0$. I_g is tunelling current through gate which has its significance at CMOS nanometer technologies [24]. In (15) C_L is load capacitance, and f is operating frequency.

Besides P_S and P_d in CMOS circuits, there is a dissipation which is a consequence of conductance of transistors, or both transistor networks in transition area. In (11) is shown that for linear excitation, in strong inversion regime:

$$P_{dsc} = \frac{1}{3} I_{ddM} (V_{dd} - 2V_t)(t_r + t_f) f\,, \tag{16}$$

where t_r and t_f are input voltage rise and fall times, respectively, and I_{ddM} is defined with (12).

Fig. 4 shows the inverter PSPICE output voltage and power supply current response, to linear excitation in weak inversion regime. In time interval $0 < t < t_1$, short circuit dissipation is defined by:

$$P_{dscsub1} = \frac{V_{ddsub}}{T} \int_0^{t_1} I_{0n}\, \mathrm{e}^{\frac{V_i - V_t}{n\phi_t}}\, \mathrm{d}t\,. \tag{17}$$

Taking into account that $V_i = V_{ddsub}\, t / t_r$ follows:

$$P_{dscsub1} = n\phi_t I_{ddMsub} t_r f\,, \tag{18}$$

where I_{ddMsub} is defined by (13). Same dissipation value can be found in time interval $t_2 < t < t_r + t_f$, therewith in (18) t_r should be replaced with t_f. During

time intervals $t_1 < t < t_r$ and $t_r < t < t_2$, power supply current is equal to pMOS transistor current in saturated area. If inverter is symetric, total amount of short circuits dissipation is as follows:

$$P_{dscsub} = 2n\phi_t I_{ddMsub}\left(t_r + t_f\right) f. \tag{19}$$

Based on (16) and (12), it can be stated that $P_{dsc} \sim (V_{dd} - 2V_t)^3$ and combining (19) and (13) $P_{dscsub} \sim \phi_t^3 e^{-(V_t + V_{ddsub})/2}$. Short circuits dissipation ratio in strong and weak inversion regime, P_{dsc}/P_{dscsub} is between 10^5 and 10^7. For example, for $V_t = 500\,\text{mV}$, $V_{dd} = 1.5\,\text{V}$, and $V_{ddsub} = 350\,\text{mV}$, it follows that mentioned ratio has a value of $P_{dsc} / P_{dscsub} \approx 4.7 \cdot 10^6$.

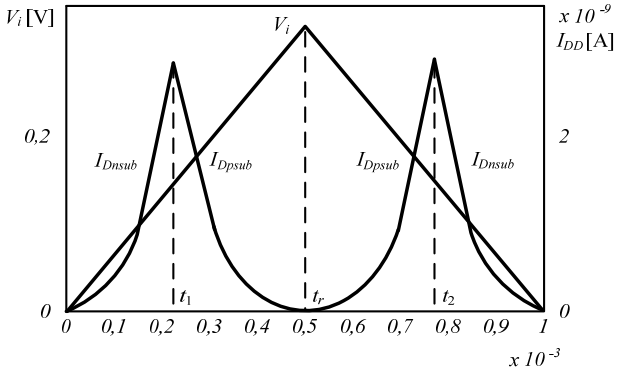


Fig. 4 – *Output voltage and supply current responses on linear excitation of CMOS inverter in weak inversion regime.*

5 Dynamic Model

Dynamic models are the same in both regimes, taking into account that values of capacitances and currents are different, because of a power supply difference. Simplified logic delay models are usually reduced to RC and models with current generator and capacitor [14, 25, 27 – 29]. Equivalent resistances or currents of current generator in CMOS strong inversion regime are dependent on saturated or non-saturated area of the characteristic. In weak inversion regime, model of current generator with constant current has been used as a function of drain-source voltage (saturated region) [14]. As it will be shown in this paper, at lower values of power supply it is not justified to ignore the influence of non-saturated switching regime.

Here, unique model, for both weak and strong inversion regime is described, with current generator whose drain current is constant through entire

switching regime. Its value is defined by $I_d - V_{ds}$ transistor characteristic in saturated region, and multiplied with correction constant whose value is dependant on power supply and transistor threshold voltage V_t. Using that constant, influence of $I_d - V_{ds}$ characteristic saturated area to transition processes can be calculated.

5.1 Delay model

MOS transistor parasitic capacitance dominantly determines the value of times in CMOS circuits' transition regime. Those are capacitance of gate towards source and drain ($C_{gsn,p}$ and $C_{gdn,p}$) of nMOS and pMOS transistor, as well as inverse polarized p-n junction drain/substrate/source capacitance ($C_{dsn,p}$).

Gate-drain capacitance $C_{gd} = C_{gdn} + C_{gdp}$ is located between output and input, and using Miller theorem it can be split and mapped to input and output. Since the variations of CMOS inverter input and output voltage are equal by amplitude, and opposite by phase, voltage gain is $A_v = -1$, so the split coefficient is equal to 2. Based on that, it can be said that all capacitance can be reduced to one input and one output capacitance, as shown in Fig. 5b, where:

$$C_i = C_{gs} + 2C_{gd} = C_{gsn} + C_{gsp} + 2(C_{gdn} + C_{gdp}), \tag{20}$$

$$C_o = C_{ds} + 2C_{gd} = C_{dsn} + C_{dsp} + 2(C_{gdn} + C_{gdp}). \tag{21}$$

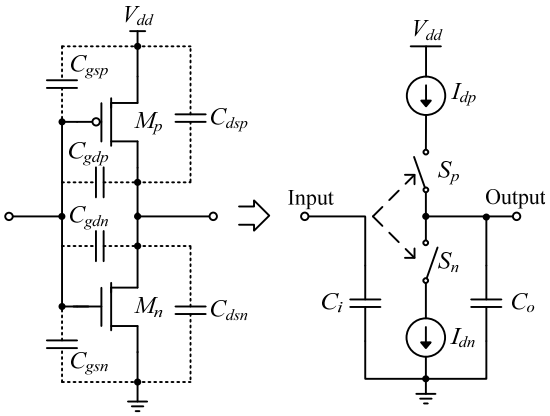


Fig. 5 – *CMOS inverter with interelectrode capacitance (a) and its dynamic model (b).*

Drain parasitic capacitance towards substrate C_{ds} include p-n junction capacitance, drain-substrate C_{jS} (F/μm^2) and peripheral capacitance source/drain C_{jp} (F/μm). Total parasitic capacitance C_{ds} (F) of transistor is:

$$C_p = C_{jS} W L_{diff} + C_{jp}\left(2W + 2L_{diff}\right), \tag{22}$$

where L_{diff} is surface drain diffusion length.

Since the charge carriers travel time between drain and source is much shorter than the charge and discharge time of capacitor, dynamic model can be represented using equivalent circuit shown in Fig. 5b. This implies instantenous on and off switching of S_n and S_p, and establishing of I_{dn} and I_{dp} currents, which are determined by static transistor characteristic $I_d - V_{ds}$. In on state of the transistor, appropriate switch (S_n or S_p) is closed, and in off state is open. I_{dn} and I_{dp} currents of current generator depends on the fact whether transistor is in saturated or non-saturated area, and has been defined with (2) in strong inversion regime, or (3) in sub-threshold regime.

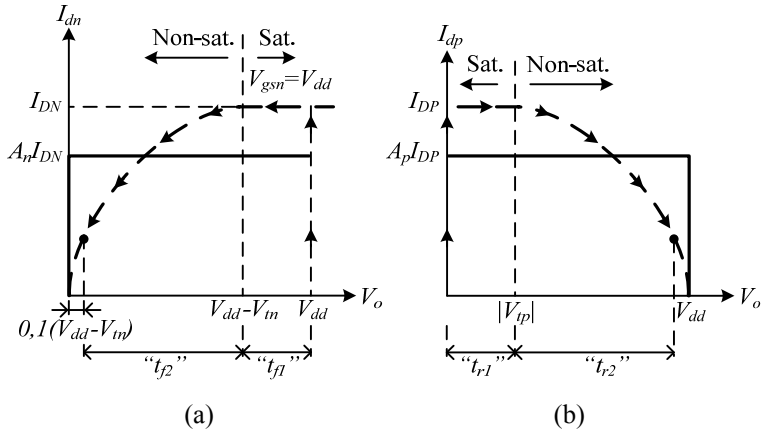


Fig. 6 – *Operating point trajectory while charging (a) and discharging of C_o (b) in strong inversion regime.*

Operating point trajectory, based on step input voltage is shown in Fig. 6 (dashed line) for strong inversion and Fig. 7 for weak inversion regime. Output voltage rise and fall time consists of two time intervals. During the first interval, on state transistor is in saturated region, while in second interval is in non-saturated region, which refers to both operating regimes. For example, changing the input voltage from 0 to V_{dd}, switch S_n (Fig. 5b) is on, and S_p is off.

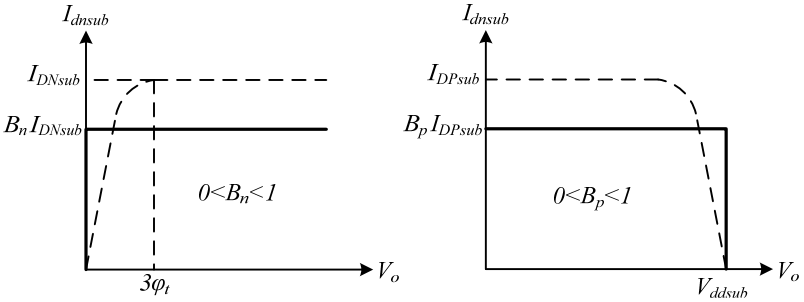
Transistor M_n operates in saturated area, and from condition $V_o(t_{f1}) = V_{dd} - V_{tn}$ we have:

$$t_{f1} = \frac{C_o}{k_n} \frac{V_{tn}}{\left(V_{dd} - V_{tn}\right)^2}. \tag{23}$$

Using the condition $V_o(t_{f2}) = 0.1 \cdot (V_{dd} - V_{tn})$, it can be stated that:

$$t_{f2} = 1.45 \frac{C_o}{k_n \left(V_{dd} - V_{tn}\right)}. \tag{24}$$

Total fall time of voltage V_o is $t_f = t_{f1} + t_{f2}$.



(a) (b)

Fig. 7 – $I_{dd} - V_i$ *model with constant currents in sub-threshold regime*

Calculation of fall and rise times can be simplified using a model with constant current across the entire switching regime. It can be accomplished by multiplying drain current in saturated region with a constant lower than 1. For example, discharge current of C_o would be (Fig. 6a):

$$I_n = A_n I_{DN} = A_n k_n \left(V_{dd} - V_{tn}\right)^2, \tag{25}$$

so that is:

$$V_o(t) = V_{dd} - \frac{1}{C_o} \int_0^t I_n \, dt = V_{dd} - \frac{A_n I_{on}}{C_o} t. \tag{26}$$

From the conditions $V_o(t_f) = 0$ and (26), it follows:

$$t_f = C_o \frac{V_{dd}}{A_n k_n \left(V_{dd} - V_{tn}\right)^2}. \tag{27}$$

A_n constant has been determined by equating (27) with the sum of (23) and (24), following that:

$$A_n = \frac{1}{1.45 - 0.45V_{tn} / V_{dd}}. \tag{28}$$

The same way, using constant current $I_{Dp} = A_p I_{dp} = A_p k_p \left(V_{dd} + V_{tp} - V_i\right)^2$ of pMOS transistor (Fig. 5b), while charging capacitor C_o, we have that output voltage rise time is:

$$t_r = C_o \frac{V_{dd}}{A_p k_p \left(V_{dd} + V_{tp}\right)^2}, \tag{29}$$

where

$$A_p = \frac{1}{1.45 + 0.45V_{tp} / V_{dd}}. \tag{30}$$

Constants A_n and A_p are dependent on $V_{tn,p} / V_{dd}$ ratio. When $V_{tn} = |V_{tp}| = V_t$, then it holds $A_n = A_p = A = 1/\left(1.45 - V_t / V_{dd}\right)$.

Procedure for determination of inverter output voltage rise and fall times in weak inversion regime is completely the same, considering that I_{dn} and I_{dp} currents are defined with (3). In this regime, boundary between saturated and non-saturated area is defined with $V_{ds} = 3\phi_t$ or $V_o = 3\phi_t$ for M_n and $V_o = V_{dd} - 3\phi_t$ for M_p.

After V_i changes from 0 to V_{dd}, capacitor C_o discharges with I_{dnsub} current of conductive NMOS transistor. In saturated region, it holds:

$$V_o(t) = V_{ddsub} - \left(\frac{I_{on}}{C_o} e^{\frac{V_{ddsub} - V_t}{n\phi_t}}\right) t, \tag{31}$$

where $V_t = V_{tn}$.

From the condition $V_o(t_{fsub1}) = 3\phi_t$ follows:

$$t_{fsub1} = C_o \frac{V_{ddsub} - 3\phi_t}{I_{on}} e^{\frac{V_t - V_{ddsub}}{n\phi_t}}. \tag{32}$$

In non-saturated region:

$$V_o(t) = 3\phi_t - \frac{I_{on}}{C_o} \int_0^t e^{\frac{V_{ddsub} - V_t}{n\phi_t}} \left(1 - e^{\frac{-V_o}{\phi_t}}\right) dt. \tag{33}$$

Differentiating (33) by time and after arranging the expression, we get the first order differential equation:

$$\int_{3\phi_t}^{V_o} \frac{\mathrm{d}V_o}{1-\mathrm{e}^{-V_o/\phi_t}} = -\frac{I_{on}}{C_o}\mathrm{e}^{\frac{V_{ddsub}-V_t}{n\phi_t}} \int_0^t \mathrm{d}t. \tag{34}$$

Considering that $e^3 >> 1$, the solution of the equation (34) is:

$$t = C_o \frac{\phi_t}{I_{on}}\mathrm{e}^{\frac{V_t-V_{ddsub}}{n\phi_t}} \left[3 - \ln\left(\mathrm{e}^{V_o/\phi_t}-1\right)\right]. \tag{35}$$

Switching regime ends when $V_o = 0$. However, for $V_o = 0$ equation (35) is indefinite. Therefore, when calculating t_{fsub2}, the same way as in strong inversion regime, we will use the fact that it is the time for which V_o reach 10% of its value at the boundary between saturated and non-saturated region, i.e. $V_o(t_{fsub}) = 0.1(3\phi_t)$. Based on that and (35), it holds:

$$t_{fsub2} \approx C_o \frac{\phi_t + 3\phi_t}{I_{on}}\mathrm{e}^{\frac{V_t-V_{ddsub}}{n\phi_t}}. \tag{36}$$

Then, output voltage total fall time is:

$$t_{fsub} = t_{fsub1} + t_{fsub2} = C_o \frac{V_{ddsub} + \phi_t}{I_{on}}\mathrm{e}^{\frac{V_t-V_{ddsub}}{n\phi_t}}. \tag{37}$$

Using simple analogy, output voltage rise time is determined by:

$$t_{rsub} = C_o \frac{V_{ddsub} + \phi_t}{I_{op}}\mathrm{e}^{\frac{V_t-V_{ddsub}}{n\phi_t}}, \tag{38}$$

where $V_t = \left|V_{tp}\right|$.

In literature, influence of non-saturated area on logic delay in weak inversion regime is ignored as a rule. Equations (37) and (38) shows that it can be justified only if $V_{ddsub} >> \phi_t$, which is fulfilled all the time. Besides thermal voltage ϕ_t which is a numerator, has influence on temperature characteristics of rise and fall times.

In weak inversion regime, constant charging and discharging currents of capacitance C_o are calculated by multiplying I_{dnsub} and I_{dpsub} of MOS transistor in saturated region, by constant $0 < B_n < 1$ (Fig. 7). In weak inversion regime, it holds that fall and rise times are, respectively:

$$t_f = C_o \frac{V_{ddsub}}{B_n I_{on}}\mathrm{e}^{\frac{V_t-V_{ddsub}}{n\phi_t}}, \tag{39}$$

$$t_r = C_o \frac{V_{ddsub}}{B_n I_{op}} \mathrm{e}^{\frac{V_t - V_{ddsub}}{n\phi_t}}, \tag{40}$$

$$B_n = B_p = \frac{1}{1 + \phi_t / V_{ddsub}}. \tag{41}$$

B_n and B_p are defined by equaling (39) with (37), or (40) with (38).

Table 2 shows calculated values of rise and fall times of inverter output voltage, as a function of power supply V_{dd}, for weak and strong inversion regime. 0.18 μm CMOS technology parameters have been used ($L_n = L_p = 0.18\,\mu\mathrm{m}$, $t_{ox} = 4\,\mathrm{nm}$, $V_{tn} = 0.366\,\mathrm{V}$, $V_{tp} = -0.37\,\mathrm{V}$, $W_n = 3\,\mu\mathrm{m}$ and $W_p = 8.5\,\mu\mathrm{m}$).

Table 2
Response times of CMOS inverter for pulse excitation as a function of power supply for strong and weak inversion regime.

	Strong inversion					Weak inversion			
V_{dd}[V]	0.8	1.2	1.5	2.2	3	0.2	0.25	0.3	0.35
t_f[ps]	28.48	12.11	8.34	4.78	3.21	554.31	187.83	61.56	19.70
t_r[ps]	22.79	9.68	6.67	3.83	2.56	443.45	150.26	49.25	15.76

It can be concluded that rise and fall times are three to five orders of magnitude lower in strong inversion, comparing to weak inversion regime.

6 NAND and NOR Circuits Optimal Geometry

Optimal geometry is symmetric structure of inverter, which implies that threshold voltages $V_{tn} = |V_{tp}| = V_t$ and MOS transistor constants k ($k_n = k_p$) are equal. From the second condition follows that for equal lengths of the channel, transistor geometry is optimal when pMOS transistor channel width is μ_n / μ_p (around 2.5) times wider than NMOS.

NAND and NOR circuits consist of dual networks (serial and parallel), containing the same number of transistors as the number of inputs. It is usual that optimal geometry is then defined according to criteria of maximum noise immunity [11]. Then, noise immunities for low and high input level are equal, and therefore we can discuss about optimal structure. However, rise and fall times, as well as output resistance in static states are different. According to these characteristics, circuit structure is asymmetric.

Static and dynamic analysis of NAND and NOR circuits can be simplified using equivalent inverter (Fig. 8). Serial transistors can be replaced with one

transistor, whose channel length is $L_{n,p}/m$, and channel width $W_{n,p}$. Similarly, parallel transistors are replaced with one whose channel length is $L_{n,p}$, and channel width $mW_{n,p}$ [11]. On the other side, influence of interelectrode capacitance can be modeled with one output capacitor whose capacitance is approximately m times larger than capacitance of one pair CMOS transistors (Fig. 9). Replacing C_o with mC_o, W_p with mW_p, and L_n with L_n/m at NANDm in (27) and (29), or W_p with W_p/m and L_n with mL_n at NORm logic circuits in (39) and (40) and equaling $t_r = t_f$, we have optimal geometry conditions as follows:

$$\text{NAND}m: \quad \frac{W_n/L_n}{W_p/L_p} = m^2 \frac{\mu_p}{\mu_n}, \tag{42}$$

$$\text{NOR}m: \quad \frac{W_n/L_n}{W_p/L_p} = \frac{1}{m^2} \frac{\mu_p}{\mu_n}. \tag{43}$$

Equations (42) and (43) refer to both strong and weak inversion operating regimes.

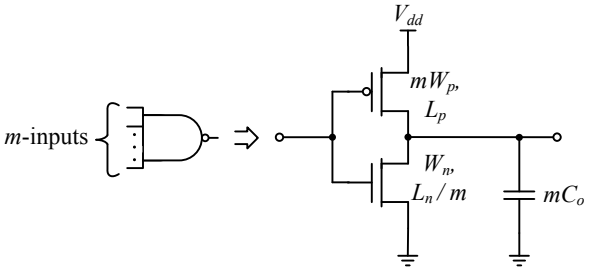
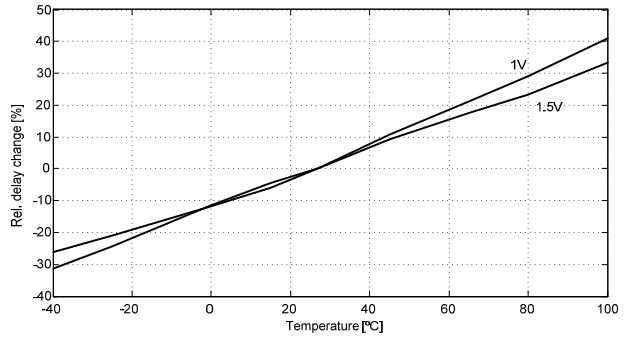


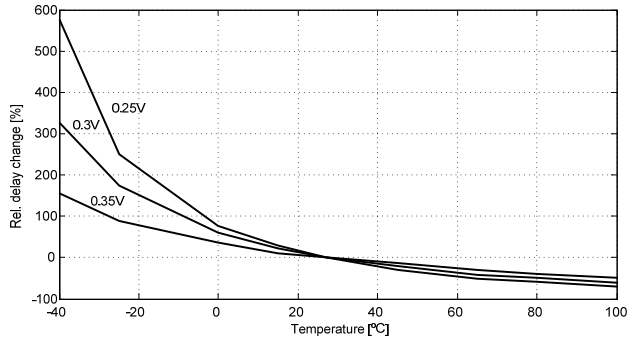
Fig. 8 – *Equivalent inverter NANDm.*

7 Temperature Characteristics

Logic threshold voltage temperature coefficient in all regimes can be lower, greater or equal to zero. It depends on transistor geometry ratio. When CMOS inverter transistors are symmetrical, threshold voltage in both strong and weak inversion regime does not depend on temperature. Logic delay temperature changes in weak inversion regime are much higher (Fig. 9) then in strong inversion regime. In temperature range from –40°C to 100°C, logic delay relative change in strong inversion regime is plus/minus few tenths of percent. In weak inversion regime, this range is from several hundreds of percent in plus, comparing to few tenths of percent in minus.



(a)



(b)

Fig. 9 – *Symetric CMOS inverter delay relative change dependant of temperature, for power supply voltage in strong (a) and weak (b) inversion regime, at* $C_L = 20\,\mathrm{fF}$.

8 DT-CMOS Logic

Equations (37) and (38) shows that delay times in weak inversion regime exponentially decreases with decrease of threshold voltage V_t. However, decrease of V_t results with increase of static consumption because sub-threshold current increases as well. CMOS logic with dynamic MOS transistor threshold (DT-CMOS) can be a good compromise [17]. Transistor bases of DT-CMOS inverter are connected to gate, instead of a source (Fig. 10).

Threshold voltage of MOS transistor is defined by

$$V_t = V_{t0} + \gamma\left(\sqrt{2\Phi_F - V_{bs}} - \sqrt{2\Phi_F}\right), \tag{44}$$

where: V_{bs} is base-source voltage, V_{t0} – threshold voltage when $V_{bs} = 0$, γ is base polarization coefficient, and Φ_f – Fermi potential. Since $V_{bsn} = V_i$, and

$V_{bsp} = V_i - V_{dd}$, threshold voltages of DTnMOS and DTpMOS transistors depend on input voltage. For $V_i = 0$, $V_{tn} = V_{t0}$, and at $V_i = V_{dd}$, with respect to (44), we have $V_{tn} < V_{t0}$. In off state, DTnMOS transistor threshold voltage is the same as with nMOS, so the static power consumption is at same level. In on state ($V_i = V_{dd}$), DTnMOS threshold voltage is lower that nMOS transistor threshold voltage. With respect to that and considering (3), we have that DT-CMOS inverter discharge current of C_L capacitor is higher, resulting lower discharge time. The same conclusion is reached for DTpMOS threshold voltage and current, while $|V_{tp}| = V_{t0}$ for $V_i = V_{dd}$, and $|V_{tp}| < V_{t0}$ for $V_i = 0$.

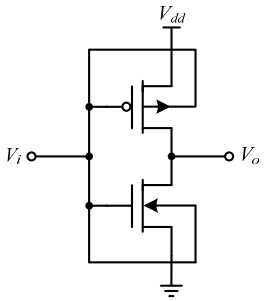


Fig. 10 – *DT-CMOS inverter.*

Given that in on state, threshold voltage and sub-threshold current of DT-CMOS transistor is equal to those in CMOS transistor, and I_d current is higher, we have that DT-CMOS inverter logic delay is lower than in CMOS one, at equal static consumption. Fig. 11 shows logic delays of DT-CMOS and CMOS inverter as a function of supply voltage V_{dd} and load capacitance C_L as parameters. For the same value of V_{dd} and C_L, DT-CMOS logic delay is several times lower comparing to CMOS inverter.

Beside increased speed, DT-CMOS inverter has improved temperature characteristics. Fig. 12a shows relative changes of threshold voltage, while Fig. 12b presents DT-CMOS and CMOS inverter logic delays as a function of temperature and supply voltage V_{dd}, at $C_L = 20\,\text{fF}$.

It should be stated that inverter supply voltage V_{dd} in Fig. 11 is limited by threshold voltage of base-source p-n junction ($V_{dd} < V_{Dt} \approx 0.6\,\text{V}$). In other words, DT-CMOS logic operates only in weak inversion regime.

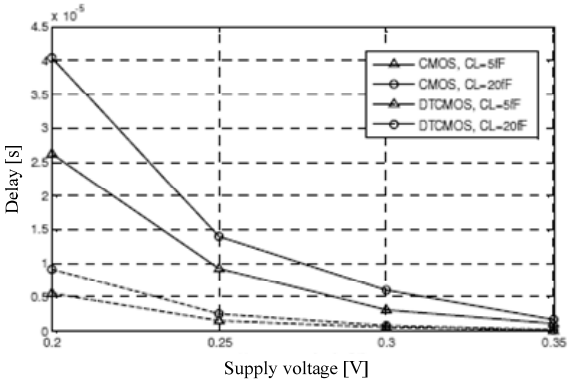
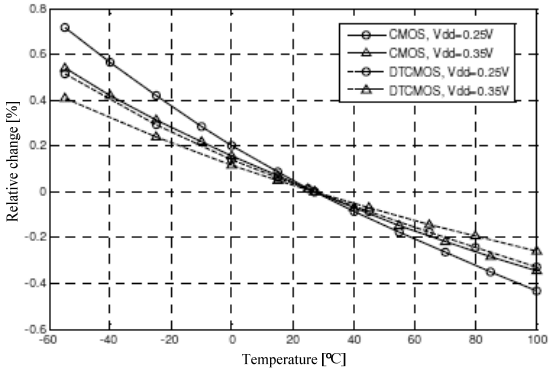
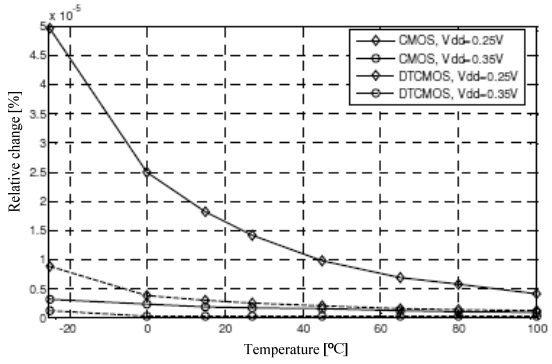


Fig. 11 – *SPICE characteristics of symetric DT-CMOS and CMOS inverter delays.*



(a)



(b)

Fig. 12 – *SPICE temperature characteristics of DT-CMOS and CMOS inverter: relative change of threshold voltage V_t (a) and logic delays (b).*

9 Conclusion

There are three CMOS operating regimes, depending on power supply voltage V_{dd} and MOS transistor threshold voltage V_t. Weak inversion regime is located in range $3\phi_t < V_{ddsub} < V_t$, mixed inversion in range $V_t < V_{ddm} < 2V_t$, and strong inversion holds for $V_{dd} > 2V_t$. Logic circuits standard topologies are completely the same in all three regimes, with complete analogies of behavior and basic parameters determination.

From drain current square dependence on input voltage in strong inversion regime, follows that threshold voltage depends on square root ratio of transistors geometry. In weak inversion regime, that dependence is logarithmic, because drain current is exponential function of input voltage.

Electrical energy consumption in weak inversion regime is several orders of magnitude lower than in strong inversion regime. Conversely, logic delay is for 4 to 6 orders of magnitude higher. Power consumption and delay in mixed regime are between weak and strong inversion.

Logic threshold voltage temperature coefficient in all regimes can be higher, lower or equal to zero, which depends on transistor geometry. Symetric inverter threshold voltage does not depend on temperature. Delay temperature characteristics in weak inversion regime are very poor, and they can be improved by applying CMOS logic with dynamic threshold (DCMOS). DT-CMOS logic is possible only in weak inversion regime.

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