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Performance Evaluation of High Speed Compressors for High Speed Multipliers

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Abstract: This paper describes high speed compressors for high speed parallel multipliers like Booth Multiplier, Wallace Tree Multiplier in Digital Signal Processing (DSP). This paper presents 4-3, 5-3, 6-3 and 7-3 compressors for high speed multiplication. These compressors reduce vertical critical path more rapidly than conventional compressors. A 5-3 conventional compressor can take four steps to reduce bits from 5 to 3, but the proposed 5-3 takes only 2 steps. These compressors are simulated with H-Spice at a temperature of 25°C at a supply voltage 2.0V using 90nm MOSIS technology. The Power, Delay, Power Delay Product (PDP) and Energy Delay Product (EDP) of the compressors are calculated to analyze the total propagation delay and energy consumption. All the compressors are designed with half adder and full Adders only.

Keywords: Compressors, Adders, Delay, Power, PDP, EDP.

Introduction

With the recent trends in increasing mobility and performance in small hand-held mobile communication and portable devices, among three thrust areas i.e speed, area and power, speed has become one of the emphases in modern VLSI design. Parallel multipliers can be used to speed up the processors comparative serial multipliers.

There are two basic approaches to enhance the speed of parallel multipliers, one is the Booth algorithm and the other is the Wallace tree compressors or counters. But as per as power concern these two methods are not suitable, energy dissipation will be more [1].

Multiplier architecture can be divided into three stages, a partial product generation stage, a partial product addition stage and final addition stage. Multipliers require high amount of power and delay during the partial products addition. For higher order multiplications, a huge number of adders or compressors are used to perform the partial product addition [2]. The number of adders was minimized by introducing different high order compressors. Binary

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counter property has been merged with the compressor property to develop high order compressors such as 5-3, 6-3 and 7-3 compressors [3, 4].

The paper is organized as follows: Section 1 is the introduction of the compressors. Wallace tree and compressors description is given in Section 2. A review of Adders is discussed in Section 3. The architectures of the compressors are discussed in Section 4. Section 5 deals with results and discussions. Finally conclusion of the paper is given in Section 6.

2 Wallace Tree

Speed is not an issue in the multipliers, the partial products can be added serially to reduce the design complexity. In high-speed designs for example 16 bit [5], the Wallace tree method [6] is usually used to add the partial products. In this method all the bits in each column at a time compresses them into two or three bits. Adders and compressors can be used to vertical bits compression in partial product reduction. An adder itself a compressor that is it compresses three bits into two bits. Hence it is a 3-2 compressor. For high order multiplication, high order compressors are used to compress the bits [7-8]. In [3], 16×16 bit multiplication is as shown in Fig. 1. 4-3, 5-3, 6-3 and 7-3 compressors are designed with half adders, full adders and a logic block is used in vertical compression of the bits. But the proposed compressors are designed with complete efficient half adders and full adders which are discussed in later sections.

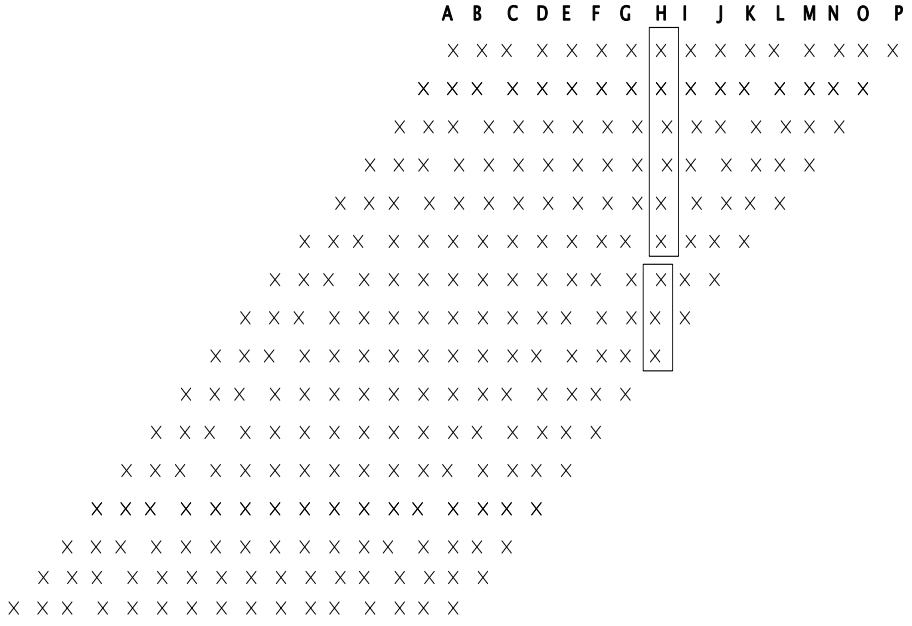

Fig. 1 – 16×16 *bit Wallace Tree multiplier*.

3 A Review of Adders

A. Half Adder: A half adder can be construct with one AND and one XOR gate. In this paper an efficient low power design is used to construct XOR gate [9].

B. Full Adder: The 1-bit full-adder functionality can be summarized by the following equations, given the three 1-bit inputs A, B, and C_{in}, it is desired to generate the two 1-bit outputs Sum and Cout, where:

$$Sum = (A \oplus B) \oplus C_{in}, \tag{1}$$

$$C_{out} = AB + C_{in}(A \oplus B). \tag{2}$$

A transmission function full adder (TFA) based on the transmission function theory is shown in Fig. 2. A transmission-gate adder (TGA) using CMOS transmission gates is shown in Fig. 3. Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a pMOS transistor and a nMOS transistor in parallel, which are controlled by complementary control signals. Both the pMOS and nMOS transistors will provide the path to the input logic "1" or "0," respectively, when they are turned on simultaneously [10]. The 14-T full adder shown in Fig. 4 design uses only one inverter, but has the problem of output glitches and sub threshold leakage power component. This is due to the incomplete voltage swing of the XOR gate output signal (an internal node of the adder) for the case $A = B = 0$, where the PMOS transistor will be ON while the NMOS will not be totally OFF, leading to a larger subthreshold current. Another 16-T full adder [11], shown in Fig. 5 uses the low power designs of XOR and XNOR gates along with pass transistors and transmission gates. The adder offers higher speed and lower power consumption than other implementations of the full adder. However, $A = B = 1$. Pass Transistor Logic based Static Energy-Recovery Full (SERF) adder with ten transistors claimed superiority in energy consumption shown in Fig. 6 [12].

The performances of the adders are verified with 90 nm technology in terms of average power, propagation delay, PDP and EDP. The results of theses adders are generated at a supply voltage $V = 2.0\,\mathrm{V}$. With the use of 16-T better results can be achieved.

Table 1

Comparison of power, delay, PDP*,* EDP *of Adders*.

Adder Type	Power [W]	Delay [s]	PDP	EDP [Js]
14-T	2.33E-05	8.97E-10	2.09E-14	1.87E-23
16-T	1.36E-05	5.07E-10	6.89E-15	3.49E-24
TFA	3.05E-05	2.51E-09	7.65E-14	1.92E-22
TGCMOS	5.07E-05	9.36E-10	4.74E-14	4.44E-23
SERF	9.04E-06	1.65E-09	1.49E-14	2.46E-23

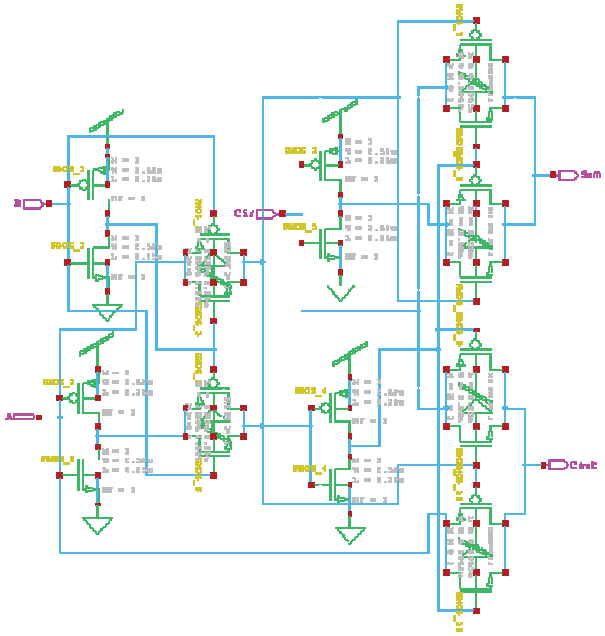

Fig. 2 – TG CMOS *Adder*.

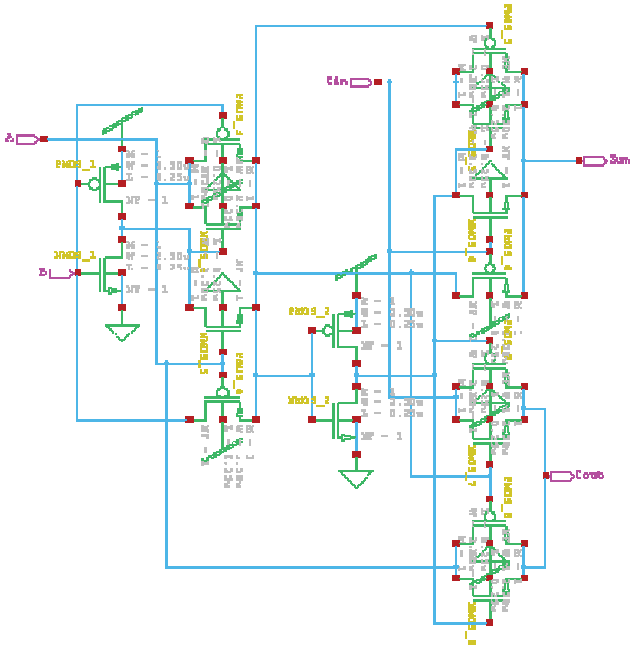

Fig. 3 – TFA *Adder*.

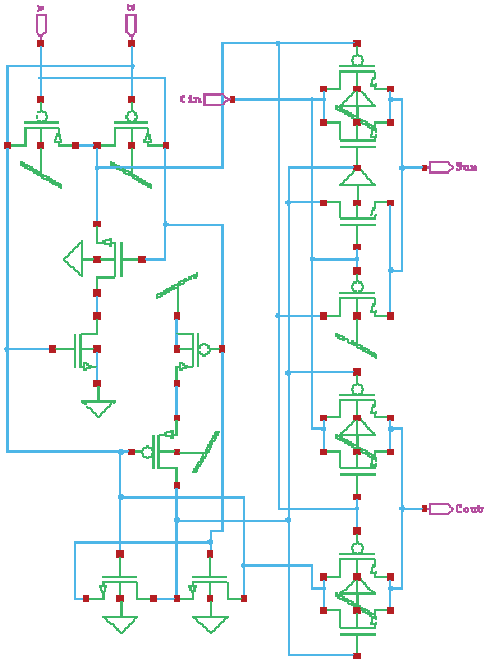

Fig. 4 – 16-T *Adders*.

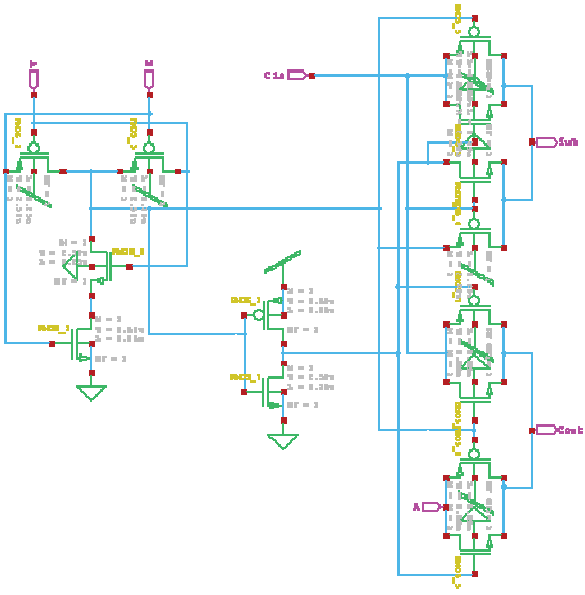

Fig. 5 – 14-T *Adder*.

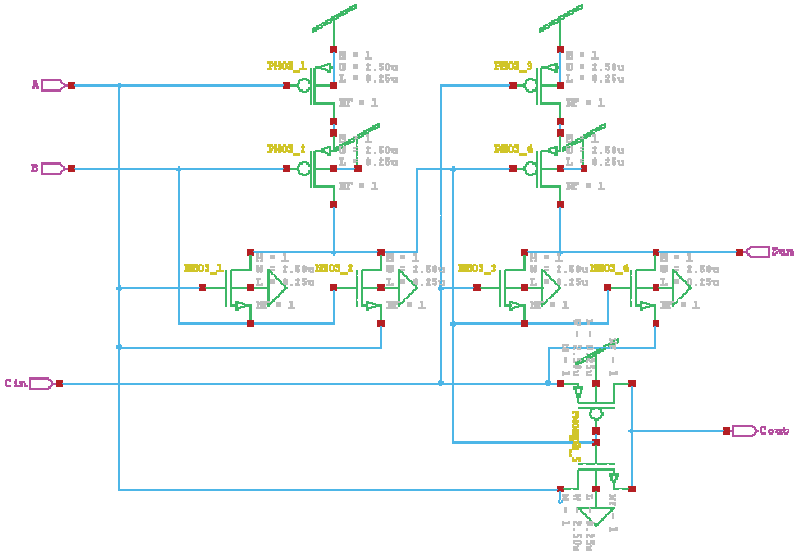

Fig. 6 – SERF *Adder*.

4 Compressor Architectures

A single bit full adder can be considered as a counter; A, B, C & D are inputs of a counter 4 and the three outputs are X, Y and Z then X is the LSB and Z is the MSB. Input combinations and the corresponding decimal count are shown in **Table 2**. Based on property of counter a compressor 4-3 as shown in Fig. 7 is constructed using a full adder and two half adders along with efficient XOR designs.

Table 2
Adder as 4, 3 *counter*.

Input	Outputs			Decimal Count
	Z	Y	X	
All the inputs are zero	0	0	0	0
Any one input is one	0	0	1	1
Any two inputs are one	0	1	0	2
Any three inputs are one	0	1	1	3
All the inputs are one	1	1	1	4

Compressor 5-3 uses 2 full adders connected with ripple type shown in Fig. 8. The compressor 6-3 uses 3 full adders and one half adder and 7-3 compressor uses 4 full adders shown in Figs. 9 and 10. Now consider the column H where there are 9 bits, to compress the column a 6-3 compressor and one full adder is needed to reduce the bits shown in Fig. 1. In column D there are 13 bits, using just one 6-3 and one 7-3 compressors we may compress them into 6 bits. Hence the multiplication will be very fast due to reduction in critical path with these compressors. The truth table of 4-3 compressor is as shown in **Table 2**.

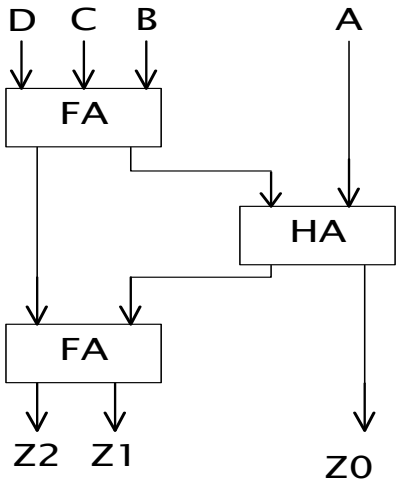

Fig. 7 – 4-3 *compressor*.

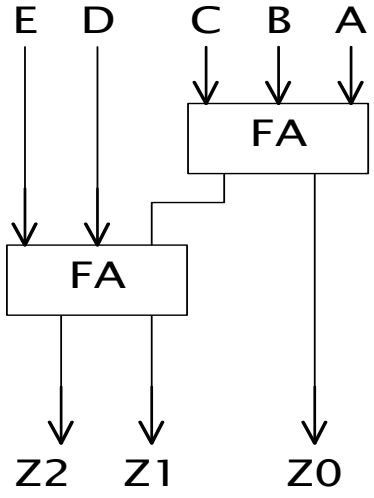

Fig. 8 – 5-3 *compressor*.

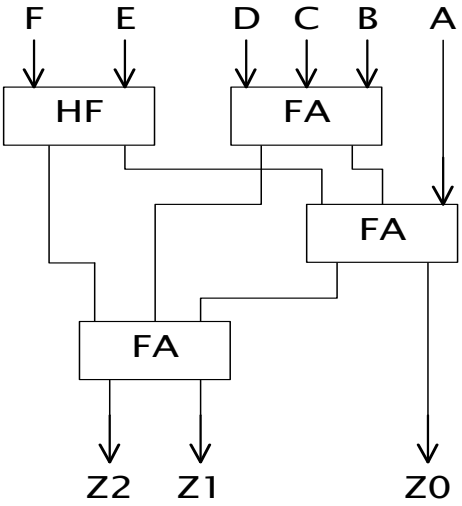

Fig. 9 – 6-3 *compressor*.

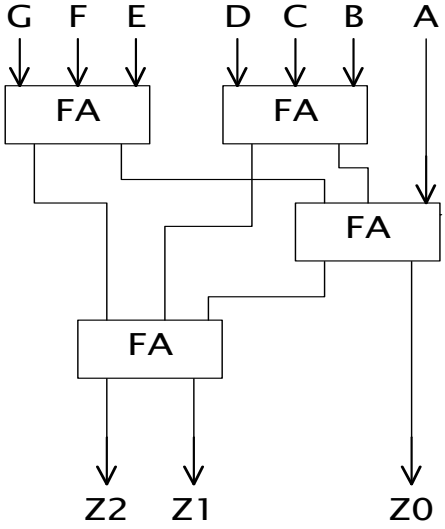

Fig. 10 – 7-3 *compressor*.

5 Results and Discussions

The functionality of the compressors is verified using Xilinx ISE 9.1 synthesis tool at gate level describing them with Verilog HDL. The simulation waveforms of these compressors are shown in Figs. 11, 12, 13 and 14.

The average power, propagation delay, Propagation Delay Product (PDP) and Energy Delay Product (EDP) of the compressors are calculated at transistor level using H-Spice with different full adder designs at a temperature of 25°C, 100MHz frequency using 90 nm MOSIS CMOS technology file. The concentration is not only on the speed, power also consider that is why power efficient XOR design is introduced in half adder to design 4-3 and 6-3 compressors. Monte-Carlo simulation has been used in the simulation for better results.

Total average powers of the proposed compressors are given in **Table 3** and the comparison graph is shown in Fig. 15. Total power includes dynamic, static and leakage power. Leakage power domination starts from nanometer technology. The total propagation delays of the compressors with the adders are shown in **Table 4** and comparison graph is shown in Fig. 16. The delay is calculated for all input and output combinations. Worst case delays of the compressors are compared. As per as power concern SERF and 16-T compressors shows better results. In the case of speed 14-T compressors had shown better performance. The power delay product in 7-3 and 6-3 TFA compressors show little economic than 16-T compressors, in remaining the 16-T compressors are the most energy efficient. The PDP comparisons of the compressors are shown in **Table 5** and comparison graph is shown in Fig. 17. Energy Delay Product (EDP) comparison is given in **Table 6** and the variation is shown in Fig. 18. In PDP and EDP 16-T and SERF compressors shown improvement than other compressor adders. The output voltage swing in 16-T compressors is also better than 14-T and SERF compressors.

Table 3

Average power (*in* [W]) *of compressors.*

Compressor Type	TG CMOS	TFA	16-T	14-T	SERF (10T)
7 - 3	4.7562E-04	2.5090E-04	7.3960E-05	7.1241E-05	4.6221E-05
6 - 3	5.1638E-04	2.2965E-04	9.8845E-05	2.7021E-04	7.3254E-05
5 - 3	2.4322E-04	1.2191E-04	3.1278E-05	3.4854E-05	1.9450E-05
4 - 3	1.3685E-03	8.3446E-04	5.0348E-04	7.2032E-04	4.0577E-04

Table 4

Delay (*in* [s]) *of the compressors*.

Compressor Type	TG CMOS	TFA	16-T	14-T	SERF (10T)
7 - 3	1.0763E-09	1.0603E-09	1.0578E-09	1.0043E-09	1.0431E-09
6 - 3	1.0835E-09	1.0674E-09	1.0583E-09	9.9821E-10	9.9129E-10
5 - 3	1.0984E-09	1.0942E-09	9.7639E-10	9.6992E-10	1.0174E-09
4 - 3	9.0469E-10	4.4560E-09	4.5822E-10	4.5102E-09	4.4632E-09

Table 5
PDP *of the compressors.*

Compressor Type	TG CMOS	TFA	16-T	14-T	SERF (10T)
7 - 3	5.1191E-13	2.6603E-13	7.8235E-14	7.1547E-14	4.8213E-14
6 - 3	5.595E-13	2.4513E-13	1.0461E-13	2.6973E-13	7.2616E-14
5 - 3	2.6715E-13	1.3339E-13	3.054E-14	3.3806E-14	1.9788E-14
4 - 3	1.2381E-12	3.7184E-12	2.2435E-12	3.2488E-12	1.811E-12

Table 6
EDP (*in* [Js]) *of the compressors.*

Compressor Type	TG CMOS	TFA	16-T	14-T	SERF (10T)
7 - 3	5.5097E-22	2.8207E-22	8.2757E-23	7.1855E-23	5.0291E-23
6 - 3	6.0622E-22	2.6165E-22	1.1071E-22	2.6924E-22	7.1983E-23
5 - 3	2.9344E-22	1.4596E-22	2.9818E-23	3.2789E-23	2.0133E-23
4 - 3	1.1201E-21	1.6569E-20	1.028E-21	1.4653E-20	8.083E-21

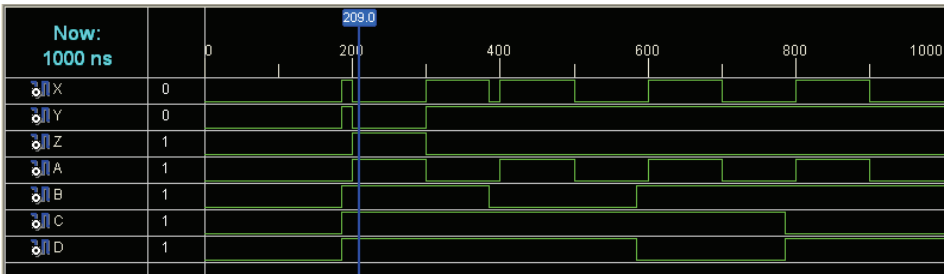

Fig. 11 – *Waveforms of* 4-3 *compressor*.

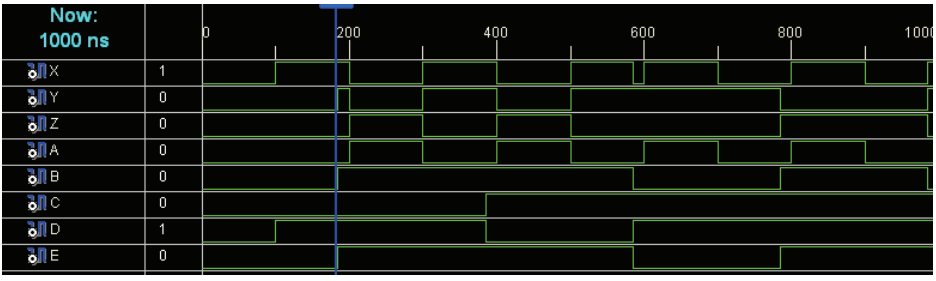

Fig. 12 – *Waveforms of* 5-3 *compressor*.

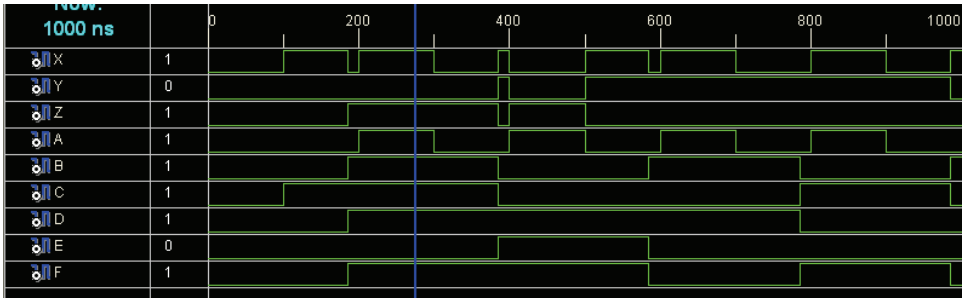

Fig. 13 – *Waveforms of* 6-3 *compressor*.

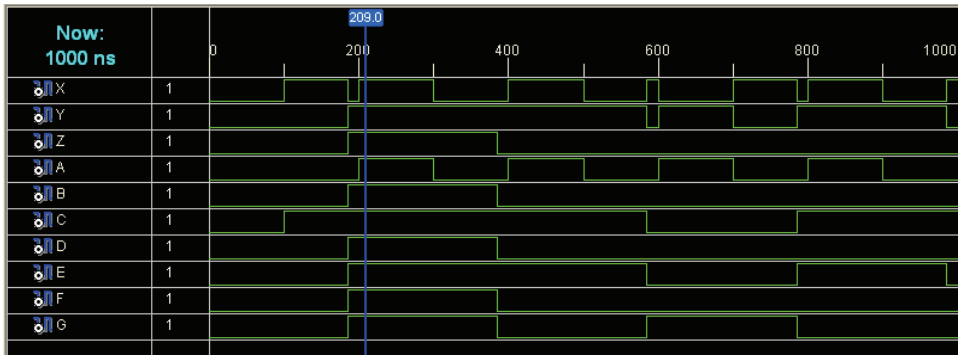

Fig. 14 – *Waveforms of* 7-3 *compressor*.

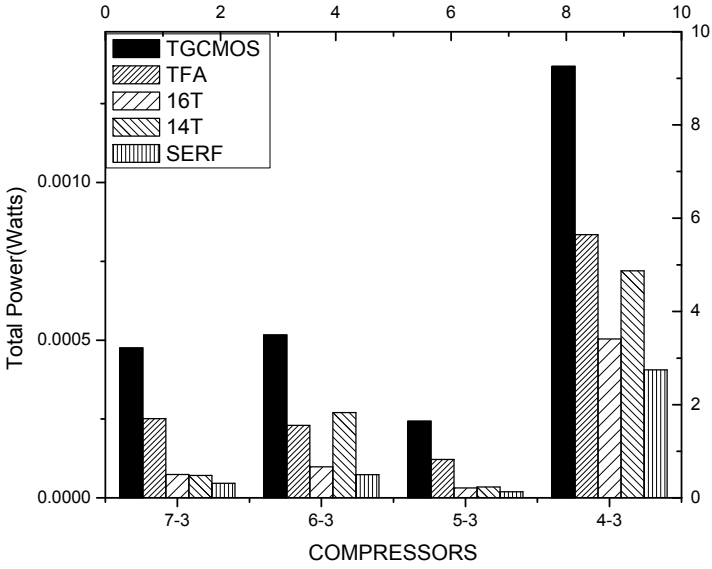

Fig. 15 – *Proposed Compressors comparison of average power*.

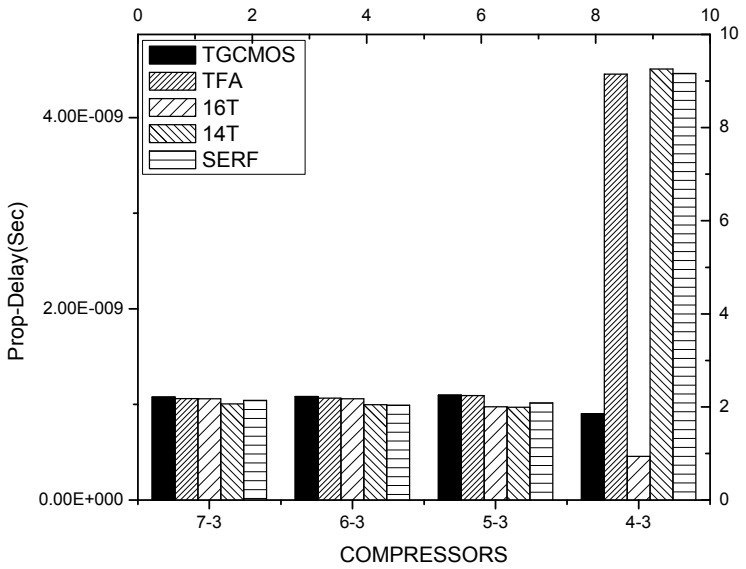

Fig. 16 – *Proposed Compressors comparison of propagation delay.*

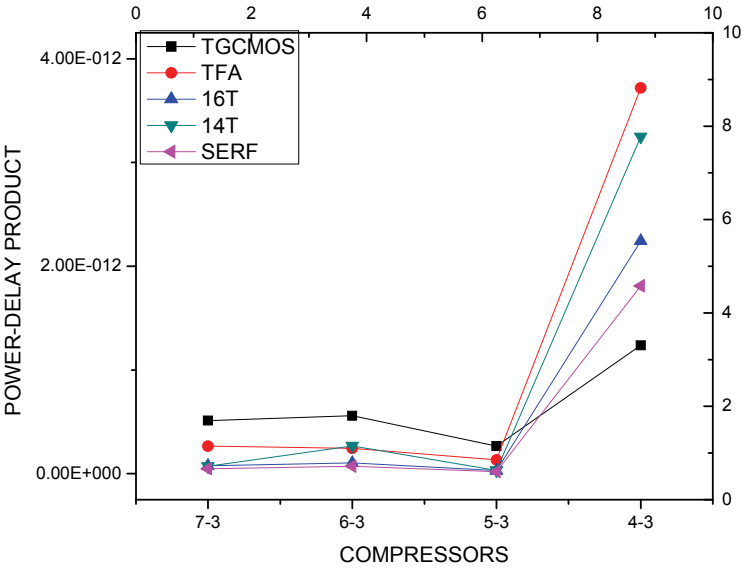

Fig. 17 – *Proposed Compressors comparison of* PDP.

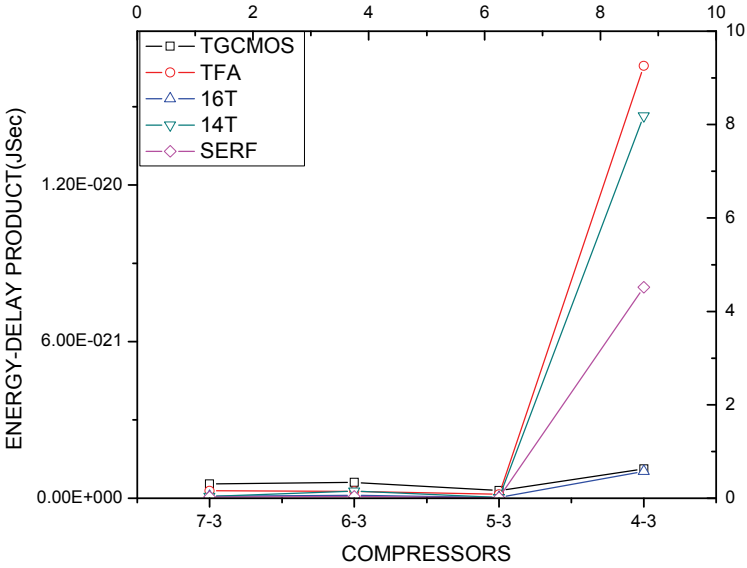

Fig. 18 – *Proposed Compressors comparison of* EDP.

6 Conclusion

To speed up Dadda, Wallace tree and Booth multipliers, compressors are the key in partial product reduction. The use of compressors in the multipliers not only reduces the vertical critical path but also reduce the stage operations simultaneously. To show better performance the compressors are tested with efficient adders. Multi threshold logic also can be use to improve the performance of the compressors. 16 bit multiplier effectively utilizes all the above said compressors for partial product reduction. The 16-T full adder compressors are the suitable for partial product reduction in multipliers than the better results of SERF. Threshold loss will be more in SERF. We can also use hybrid adders instead of using same adders to design a compressor.

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