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Influence of Current Reuse LNA Circuit Parameters on its Noise Figure*

Jelena Radić[1,a], Alena Djugova[1,b], Mirjana Videnović-Mišić[1,c]

Abstract: A 2.4 GHz low noise amplifier (LNA) with a bias current reuse technique is proposed in this work. To obtain the optimum noise figure (*NF*) value, dependence of *NF* on its most influential LNA parameters has been analysed. Taking into account the LNA design requirements for other figures of merit, values of the circuit parameters are given for the optimum noise figure.

Keywords: Low Noise Amplifier (LNA), Noise Figure (*NF*), Noise factor (*F*), Current reuse technique.

1 Introduction

Low Noise amplifier (LNA) is one of the most important blocks in the RF receiver chain. Its role is adequate amplification of the weak received signals (signal power levels are typically in the range from –110 dB to –70 dB [1]) with minimal noise contribution. The additional LNA constraint is sufficient linearity without distortion of the amplified signal. One way of satisfying all these requirements is increase in LNA gain. In this case, LNA noise and the noise contribution of the subsequent stages are decreased [2]. As direct increase in LNA gain could cause its non-stable operating it is very importantly to pay attention to the circuit stability. To prevent input and output signal reflection, it is necessary to provide good input and output impedance matching during amplifier design. The LNA input impedance matching is extremely important as it ensures very weak signal received at antenna to be grouted with less attenuation and amplified in the LNA. Output impedance matching provides normal signal flow through the receiver.

In this paper, a narrowband LNA has been proposed. To reduce current/power consumption, a current reuse technique is used. The LNA is designed using 0.35 µm SiGe BiCMOS austriamicrosystems (ae) S35D4 technology. The chosen technology offers transistor real models operating up to 6 GHz and high performance passive components (for example, inductors with

[1]Department of Power, Electronics and Communications, FTN, University of Novi Sad, 21000 Novi Sad, Serbia
E-mails: [a]jelenar_@uns.ac.rs; [b]alenad@uns.ac.rs; [c]mirjam@uns.ac.rs
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good quality factor that are essential for LNA design). Noise Figure parameter (*NF*) [3] dependence on its dominant circuit parameters have been presented and analysed. Based on results and conclusions obtained after analyzing the LNA, the optimal *NF* value has been achieved in last section.

2 The Current Reuse LNA Topology

The designed LNA, shown in Fig. 1, consists of two amplifying stages. Using the current reuse technology, one amplifying stage is placed on the top of the other. Apropos, the cascode configuration is used for LNA. With this approach, higher gain has been obtained without both, usage of the cascade configuration and increase in consumption as two amplifier stages have the same bias current ($P_D = V_{DD} I_D$). Since it is required for the LNA to have high gain and good cuircuit stability, cascode amplifier (M_1 and M_2 transistors) is the main contributor to the overall LNA gain. Besides high gain, the cascode amplifier provides high output impedance and good input to output isolation. As drain AC load of transistor M_1 in the cascode amplifier is approximately $1/g_{m2}$ (input impedance of transistor M_2, common gate CG amplifier), drain M_1 represents low impedance point. As transistor M_1 gate to drain gain is small, effect of Miller gate-drain overlap capacitance can be neglected.

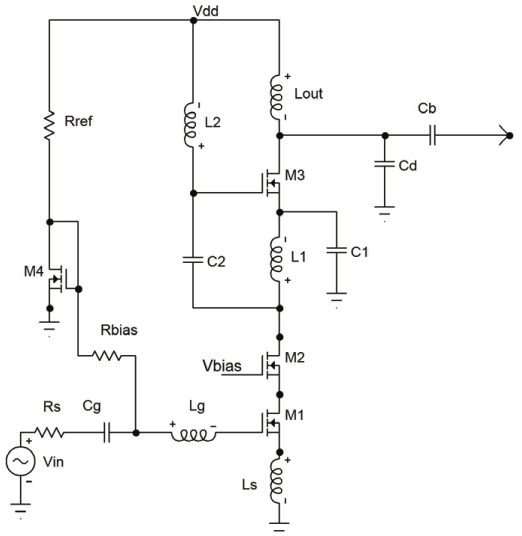


Fig. 1 – *The designed* LNA.

Additional amplifying stage (transistor M_3) has common source topology in case capacitor C_i, $i = 1,2$, is large. Resistor R_S represents source output

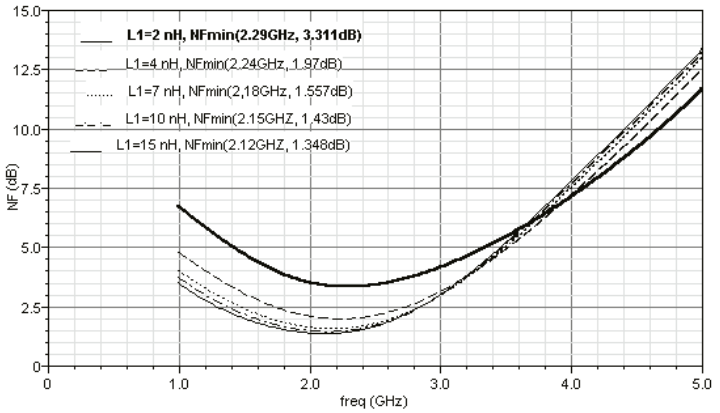
impedance (the most usual value is 50 Ω). For providing a good input matching the inductive source degeneration with inductor L_S is used [3, 4]. Additional degree of freedom, while setting resonant frequency ω_0, is introduced with inductor L_g. For predefined C_{gs1} (capacitance between gate and source) and L_S (obtained from requirement $Z_{in} = R_S$), choice of suitable L_g value results in wanted resonant frequency ω_0:

$$\omega_0 = \sqrt{1/C_{gs}\left(L_s + L_g\right)}\,. \tag{1}$$

Bias circuit consists of transistor M_4 and resistor R_{ref}. The resistor R_{bias} is chosen large enough to represent high impedance to the carrier that prevents AC signal flow to the bias circuit, giving at the same time small contribution to the overall circuit noise. Voltage V_{bias} is transistor M_2 bias voltage. Large capacitor C_1 enables coupling of two amplifier stages by transmitting signal from M_2 transistor drain to M_3 transistor gate. Moreover, capacitor C_2 should have the highest possible value to provide the ideal AC ground for the second amplifier stage. Inductors L_1, L_2 and L_{out} represent loads of first and second amplifier stage. Capacitors C_g and C_b are input and output blocking capacitors. From the LNA topology it can be seen that the total node capacitance at the drain of M_3 is paralell of capacitance C_d and transformed capacitance C_b. This equivalent capacitance forms paralell resonant circuit with inductance L_{out} both to provide highly desirable band-pass filtering of output signal and increase gain at the center frequency. At the LNA input, resonant frequency of the serial resonant circuit is usually set equal to output resonant frequency. But, if desired, these resonances can be offset from each other yielding a smaller gain, flatter and broader response.

3 Dependence of Noise Figure on its Most Influential LNA Parameters

Noise factor (*F*) describes degradation of the signal to noise ratio (S/N) through the circuit [2, 3]. However, noise figure ($NF = 10\log F$) is more often used in literature and simulators for specifying noise performance of an LNA. To examine dependence of noise figure on circuit parameters, one by one circuit parameters have been changed. The designed LNA has been simulated using Spectre Simulator from Cadence Design System with options for RF analysis. For all circuit components, except for transistors (BSIM3v3 models), ideal models are used during simulations.



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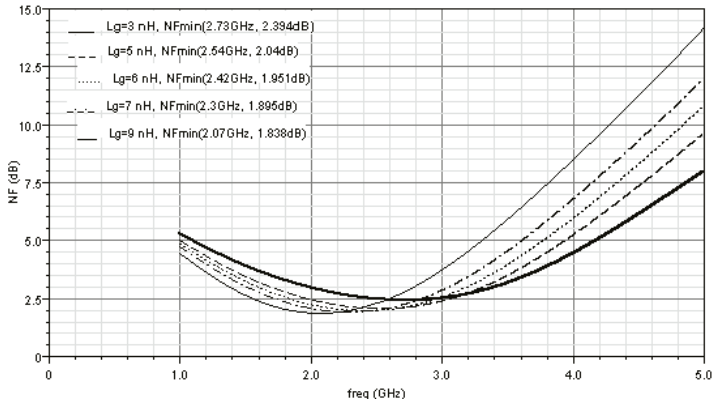

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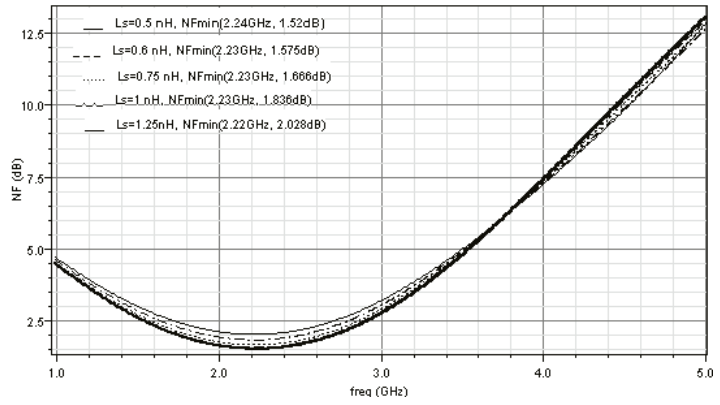
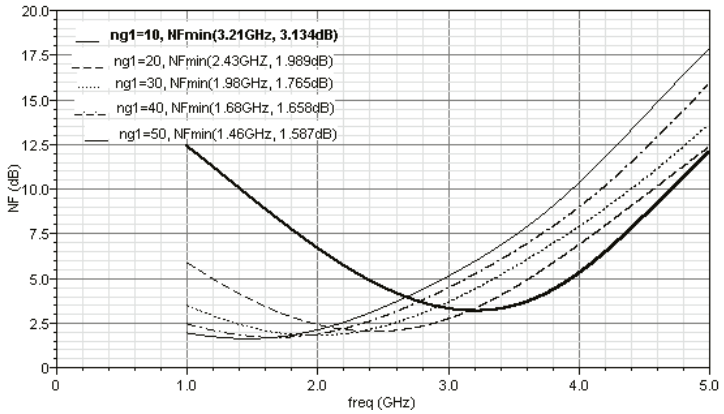
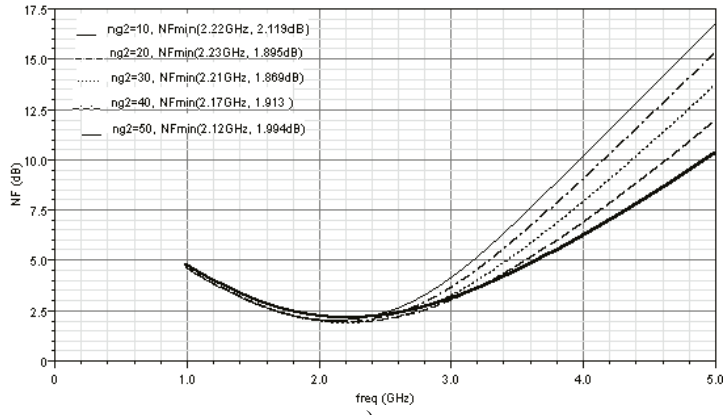


c)

Fig. 2 – *Dependence of NF on*: a) L_1; b) L_g; c) L_S;



d)



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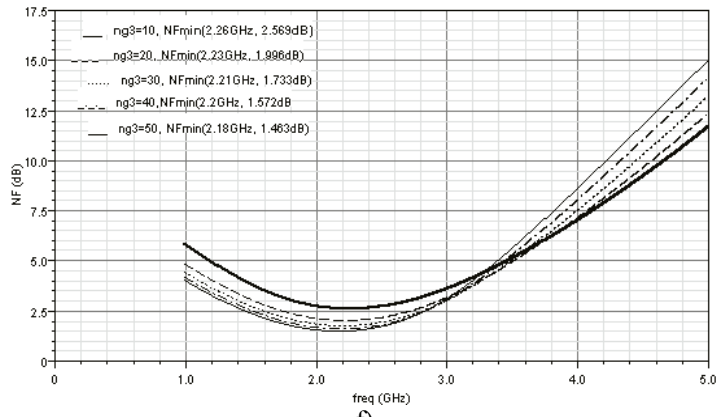
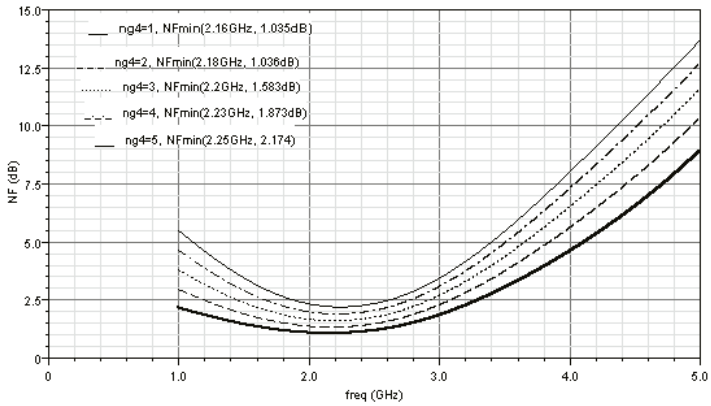
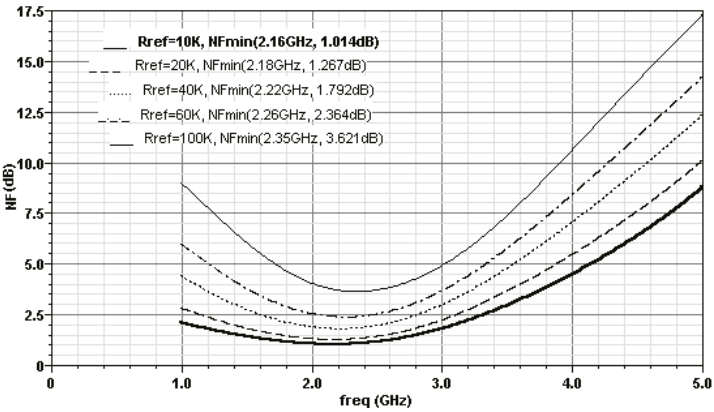


f)

Fig. 2 – *Dependence of NF on*: d) n_{g1}; e) n_{g2}; f) n_{g3};



g)



h)

Fig. 2 – *Dependence of NF on*: g) n_{g4}; h) R_{ref}.

It has been noticed that the highest influence on *NF* parameter have inductors L_1, L_2, L_g, and L_S, transistor dimensions given by n_{gi} parameter (the gate fingers number of transistor M_i, $i = 1,2,3,4$) and resistor R_{ref} (Fig. 2) [5]. Dependence of transistor M_i width on parameter n_{gi} is given by expression $W_i = 5n_{gi}$ [μm], $i = 1,2,3,4$. In the case of transistors M_1, M_2 and M_3, the right side of the W_i expression is multiplied by 4 as those transistors are made of four transistors in parallel.

If we apply procedure for derivation of the noise figure regarding only the first order effects for transistors, explained in [4], the noise factor *F* of the circuit shown in Fig. 1, will be given by:

$$F = 1 + \frac{R_{Lg} + R_g}{R_S} + \left(\frac{\omega}{\omega_t}\right)^2 \gamma_{gd01} AB + \frac{4\gamma g_{d03}\left(1 - \omega^2 L_{12} C_{gs3}\right)^2}{g_{m3}^2 \omega_t^2 L_{12}^2} A, \qquad (2)$$

where:

$$A = \frac{\left[(R_S + \omega_t L_S)^2 + \left(\omega L_S + \omega L_g - \frac{1}{\omega C_{gs1}}\right)^2\right]}{R_S},$$

$$L_{12} = \frac{L_1 L_2}{L_1 + L_2},$$

$$B = \left| \frac{1}{\left[1 + \frac{\omega_t L_S}{R_S + j\omega(L_S + L_g) + \frac{1}{j\omega C_{gs1}}}\right]} \right|^2.$$

Resistors R_g and R_{Lg} represent resistances of the transistor M_1 gate and the inductor L_g. Since their values are negligible in regard to source resistance R_S, their contribution to the total noise figure is mostly ignored [2, 4].

The inductor L_1 influence on the noise figure is shown in Fig. 2a. Similar behavior was observed for *NF* dependence on the inductor L_2 value. This is expected due to roles of the inductors in the LNA design and their places in equation (2). From the equation (2) can be seen that inductor L_1 (L_2) affects the last component of the equation. Other parts of the sum (2) are constant with L_1 (L_2) variation at constant frequency. Increase in L_1 (L_2) results in L_{12} increase. At lower frequencies, where condition $\omega^2 L_{12} C_{gs3} \ll 1$ is valid, L_{12} increase results in reduction of the expression (2) last component. Consequently, parameters *F* and *NF* decrease. However, at higher frequencies value $\omega^2 L_{12} C_{gs3}$ increases and becomes higher than one. Therefore, noise figure increases with increase in L_{12} due to increase in the last part of the equation (2). For C_{gs3} value close to 1pF and L_{12} value in the range from 2nH to 7.5nH, this behavior can be seen in Fig. 2a for frequencies $f < 3.85\,\text{GHz}$ and $f > 3.85\,\text{GHz}$.

As the noise is transmitted from the input to the output of the circuit amplified with the total LNA gain, it is expected that components in the input circuit have the highest influence on the noise figure. Dependence of the *NF* on

inductors L_g and L_S values are given in Figs. 2b and 2c. However, these noise figure dependences are not simple for analysis. It can be seen that inductances L_g and L_S are not only in the numerator of the equation (2) last component but also in the numerator and denominator of its third component. To explain exactly how change of these inductances alters the noise figure, it is necessary to introduce exact values all of the parameters in equation (2), which wouldn't have purpose in this analysis. Intuitively observed, change of these inductor values modifies the total LNA gain and quality factor of the input resonant circuit (equations given in [3]) changing directly *NF* value. In the LNA design, the inductance L_g is higher than inductance L_S value, so the both parameters are varied according to their expected value levels.

It can be seen from Figs. 2d, 2e, and 2g that the first transistor has major contribution to the noise figure while the second transistor influence on *NF* is small (almost neglected). This behavior is expected due to positions of these transistors in the LNA topology. Theory, presented in [3, 4], describes how noise figure can be decreased by transistor scaling, namely decreasing transistor width W and reducing g_{d0} at the same time. However, at certain transistor width, further transistor scaling will cause increase in the noise factor (and the noise figure). At that point induced gate noise, inversely proportional to g_{d0} [3, 4], becomes dominant. This behavior is observed in the case of the first (and the third transistor) where reduction of W_1 (W_3) results in noise figure minimum increase, particularly for $n_{g1} = 10$ ($n_{g3} = 10$). Moreover, the noise figure minimum shifts significantly with transistor M_1 scaling as increase in W_1 decreases proportionally C_{gs1} ($C_{gs1} = 2C_{ox}L_1W_1/3$). Reduction in C_{gs1} changes directly the input resonant circuit quality factor Q which determines the noise figure minimum position [4]. For transistor M_1 simulated widths, it can be seen that the designed circuit has minimal noise figure at operating frequency for $n_{g1} = 20$. For n_{g2} values of 50, 40, and 30 (drain noise domination) transistor scaling reduces *NF* parameter, Fig. 2f). However, further reduction in W_2 increases *NF* parameter (gate noise domination) at lower frequencies. At higher frequencies, the noise figure value is lower for smaller W_2 value. Only for transistor M_4 and all simulated W_4 values, *NF* value decreases with W_4 reduction. This behavior was expected as a consequence of theory above ([3, 4]) and the fact that this transistor is part of the LNA bias circuit. Influence of transistor M_4 gate induced noise would not be seen in the total noise figure as its operating frequency is significantly lower than $0.1f_t$, which represents

frequency limit for beginning of the induced gate noise activity. As transistor M_4 determines the first transistor bias, it's necessary to mention that change of W_4 alters not only the total noise generating by this transistor, but also voltage V_{GS1} [5]. With transistor M_4 scaling V_{GS1} and LNA gain are increased, resulting in noise figure decrease.

As resistor R_{ref} represents part of bias circuit, resistance increase results in decrease of voltage V_{GS1} and LNA gain. Consequently, noise factor (noise figure) is increased (shown in Fig. 2h).

4 The Optimum Noise Figure Value

Initial device dimensions and component values (of the circuit shown in Fig. 1) were obtained using the optimization technique with constant power consumption [2, 4] at 2.4 GHz operating frequency. The initial simulation result for *NF* parameter, with calculated LNA parameter values, was 1.933 dB. The optimum noise figure value was achieved after analyzing *NF* dependence on circuit parameters and is 1.137 dB at 2.4 GHz, Fig. 3.

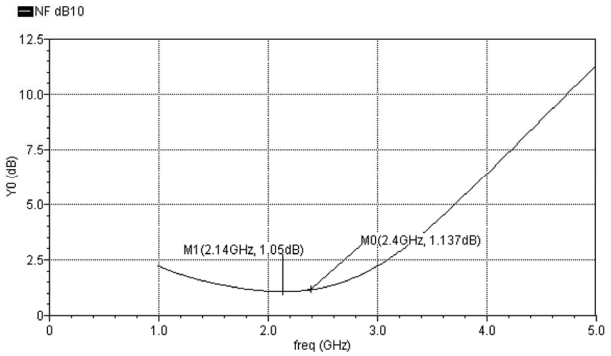


Fig. 3 − *The optimum NF value.*

It can be seen from Fig. 3 that obtained value is very close to the minimum *NF* value ($NF_{\min} = 1.05\,\text{dB}$ at 2.05 GHz frequency). It is necessary to emphasize that *NF* value was obtained taking into account values for other LNA figures of merit, especially S parameters [2]. The noise figure could be even lower if the other LNA design requirements, given in Section 1, were not satisfied. Component initial values and values for the optimum noise figure were given in **Table 1**. This table shows that the highest differences between the initial and the optimum value are for transistor M_3 width (given by parameter n_{g3}), inductors L_1 and L_2 values whose increase significantly reduces noise figure.

Although *NF* dependence on LNA parameters analysis showed that transistor M_3 scaling increases *NF*, n_{g3} value was decreased to satisfy requirements for other LNA figures of merit. Better *NF* value could be achieved by further transistor M_4 scaling (n_{g4} value was decreased from 4 to 3). In that case LNA gain performance would be degraded and additional problem in device fabrication would be introduced (for $n_{g4}=3 \Rightarrow W_4=15\,\mu\text{m}$). Resistor R_{ref} initial value was not changed as R_{ref} increase could considerably reduce *NF* parameter together with significant increase in power consumption.

Table 1
The component initial values and values for the optimum noise figure.

Component	Initial value	Optimum value
L_1	4.3976 nH	13.135 nH
L_2	4.3976 nH	13.135 nH
L_g	7.5984 nH	6.8823 nH
L_S	1.0501 nH	641.672 pH
$n_{g1}\,(M_1)$	24	24
$n_{g2}\,(M_2)$	24	24
$n_{g3}\,(M_3)$	24	10
$n_{g4}\,(M_4)$	4	3
R_{ref}	42.9 kΩ	42.9 kΩ

5 Conclusion

In this paper, dependence of noise figure on current reuse low noise amplifier parameters has been analyzed. Simulation results were showed that *NF* was dominantly influenced by inductors L_1, L_2, L_g and L_S, all transistors widths, and resistor R_{ref}. Results also demonstrated that the highest decrease in *NF* can be obtained by increasing inductors L_1 and L_2. Using analysis results and considering requirements for the other LNA figures of merit, the $NF=1.137\,\text{dB}$ optimum value was achieved.

6 Acknowledgment

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