SERBIAN JOURNAL OF ELECTRICAL ENGINEERING
Vol. 6, No. 2, November 2009, 215-225

UDK: 681.515:621.314.1

A DSPIC Implementation of a Sliding Mode Strategy for a SEPIC Converter

Arivukkannu Ezhilarasi[1], Muthiah Ramaswamy[2]

Abstract: This paper attempts to implement an elegant Variable Structure Controller (VSC), with a view to regulate the output voltage and improve the power quality of input current of a Single-Ended Primary Inductance Converter (SEPIC) through the use of a DSPIC processor. It aims to exploit the advantages of ease of implementation and robustness of VSC, which facilitates to produce an output that is independent of input voltage, circuit parameters and/or output load. The DSPIC card is designed to perform the function of a VSC, besides serving to generate trigger pulses for the power switches. Simulation and experimental results are presented to demonstrate the merits of the proposed approach.

Keywords: VSC, DSPIC, Voltage regulation, Time response, Power quality.

1 Introduction

DC-DC converters are popularly used with switch mode power supplies. They exhibit complex dynamic behaviour due to their nonlinear nature, resulting from repeated switching operation [5,15]. The Single-Ended Primary Inductance Converter (SEPIC) has become a popular topology that finds applications in distributed power systems and battery chargers. However there is still considerable scope for improvement in its time response characteristics and enhancement of power quality.

The SEPIC structure is consisted of two inductors, two capacitors and a diode in its configuration. It produces output voltages that are lower or higher than the input voltage and also of the same polarity as the input voltage in contrast with the boost, buck-boost and CUK converters. The dc blocking capacitor in the power path offers some degree of isolation between the input and output voltages, thereby protecting the complete system. The switching voltages are clamped by capacitors, so that the ringing caused by the leakage inductance is of little or no consequence in a SEPIC converter. The input

[1]Department of Electrical Engineering, Annamalai University, Annamalai Nagar-608002, South India;
E-mail: jee.ezhiljodhi@yahoo.co.in
[2]Department of Electrical Engineering, Annamalai University, Annamalai Nagar- 608002, South India;
E-mail: aupowerstaff@gmail.com

inductor serves to avoid a pulsating input current as in the case of a conventional buck boost converter.

A small signal model for a current mode controlled SEPIC converter has been developed [14]. A current controlled PWM switch model based on the average large and small signal models of a current programmed SEPIC converter to operate in continuous conduction mode has been built [11]. A dynamic model of a non-isolated and isolated SEPIC converter has been proposed [8]. An average switch model to represent the power devices has been suggested [3]. A posicast controller has been designed for a DC-DC buck converter in order to lower the noise in the control signal [9].

An improved power quality has been found to significantly relieve the burden of the input ac source. The most commonly used power factor (PF) correction circuit has been the boost PF pre-regulator. However, the main disadvantage of the boost converter has been that the output voltage tends to be higher than the input voltage over the entire input range [1,4]. A continuous conduction mode SEPIC converter has been proposed for power factor correction [6]. A new topology of SEPIC converter has been designed for power factor correction applications [13].

The control strategy has been found to greatly influence the effective operation of a SEPIC converter [7,10]. Hence it is proposed to design a control algorithm suitable for SEPIC and implement it with a state-of-the-art processor in order to achieve an improved time response and the desired power quality.

2 Problem Formulation

The objective of this paper is to model a SEPIC converter in the state space domain, build the sliding mode strategy and evaluate the performance through simulation and hardware implementation. The DSPIC processor is to be programmed to generate PWM signals for the power switch in the converter, besides performing the role of a Proportional Integral (PI)/ Sliding Mode(SM) controller. The simulated performance is to be validated through experimental results.

3 Modelling

Most modelling concepts in power electronics are mainly intended to express the nonlinear time varying phenomena in a mathematical form [2,12,16] to permit the incorporation of a suitable controller. The state space averaging method which serves to bring out explicitly the static and dynamic characteristics of the system is used to build the control algorithm.

The state matrix governing the operation of the SEPIC, with power switch on is:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_o \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{R_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R_o C_o} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in}. \quad (1)$$

With power switch off:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_o \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & -\frac{R_2}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_0} & -\frac{1}{C_0} & 0 & -\frac{1}{R_o C_o} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in}. \quad (2)$$

Using state space averaging technique the final state matrix reduces to the form:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ Vc_1 \\ V_o \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & -\frac{(1-D)}{L_1} & -\frac{(1-D)}{L_1} \\ 0 & -\frac{R_2}{L_2} & -\frac{D}{L_2} & \frac{(1-D)}{L_2} \\ \frac{(1-D)}{C_1} & \frac{D}{C_1} & 0 & 0 \\ \frac{(1-D)}{C_o} & -\frac{(1-D)}{C_o} & 0 & -\frac{1}{R_o C_o} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ Vc_1 \\ Vo \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in}. \quad (3)$$

4 Control Strategy

The desired objective is inserted into the controller through the design of a switching surface, predicted from the switching pattern. The converter is forced to switch across this sliding surface through the construction of a switching

control law, which satisfies a set of necessary conditions for the operation of the sliding mode.

The switching function is chosen to be:

$$\sigma = \begin{bmatrix} g_1 & g_2 & g_3 & g_4 \end{bmatrix} \cdot \begin{bmatrix} e_{i1} \\ e_{i2} \\ e_{Vc1} \\ e_{Vo} \end{bmatrix} = g_t E \,, \tag{4}$$

where g_1 to g_4 are constant gains and e_{i1} is error in the input inductor current:

$$e_{i1} = i_{1ref} - i_1 \,;$$

e_{i2} is error in the current of inductor L_2:

$$e_{i2} = i_{2ref} - i_2 \,;$$

e_{Vc1} is error in the coupling capacitor voltage:

$$e_{Vc1} = V_{c1ref} - V_{c1} \,;$$

e_{Vo} is error in the output voltage:

$$e_{Vo} = V_{oref} - V_o \,.$$

The input current and output voltage are measured and controlled directly. This is equivalent to setting gains g_2 and g_3 to zero. Thus the sliding surface will be:

$$\sigma = g_i e i_1 + g_v e_{Vo} \,. \tag{5}$$

The term *D* representing duty cycle in equation (3) is replaced by a variable u, such that it depends on the state of the switch.

$$u = \begin{cases} 1, & \text{when } S \text{ is } ON; \\ 0, & \text{when } S \text{ is } OFF. \end{cases}$$

Thus the overall state space model is given by:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_0 \end{bmatrix} = \begin{bmatrix} -\dfrac{R_1}{L_1} & 0 & \dfrac{u-1}{L_1} & \dfrac{u-1}{L_1} \\ 0 & -\dfrac{R_2}{L_2} & -\dfrac{u}{L_2} & \dfrac{1-u}{L_2} \\ \dfrac{1-u}{C_1} & \dfrac{u}{C_1} & 0 & 0 \\ \dfrac{1-u}{C_o} & \dfrac{u-1}{C_o} & 0 & -\dfrac{1}{R_o C_o} \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ Vc_1 \\ V_o \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \,. \tag{6}$$

The control law is expressed as:

$$u = \begin{cases} 1 & \sigma < 0 \\ 0 & \sigma > 0 \end{cases} \tag{7}$$

A necessary condition for the sliding surface to exist is:

$$g_t \cdot A_4 \le 0\,, \tag{8}$$

where g_t is the gain matrix and A_4 is fourth column of matrix A of the overall state space model at which u is set to zero. The above matrix is reduced with a view to determining the criterion for calculation of gain.

$$\frac{-g_i}{L_1} - \frac{g_v}{R_o C_o} \le 0\,. \tag{9}$$

If the sliding condition exists, then the system trajectory will move along the designed sliding surface, so long as the above two conditions are satisfied.

5 Simulation Results

The scheme is simulated using MATLAB SIMULINK. The buck/boost converter parameters are chosen as $R_1 = 0.1\,\Omega$, $L_1 = 200\,\mu\text{H}$, $R_2 = 0.2\,\Omega$, $L_2 = 510\,\mu\text{H}$, $C_1 = 47\,\mu\text{F}$, $C_o = 200\,\mu\text{F}$, switching frequency is $50\,\text{Hz}$ and allowed to a load vary up to 5000 W. A dc voltage of 350 V obtained through a front end rectifier is applied to the buck/boost converter. The reference outputs are fixed at 230 V for buck converter and 440 V in the case of boost converter.

The output voltage and current corresponding to a load of 1 kW for both buck and boost modes of the SEPIC are depicted in Figs. 2 and 3. Sudden changes in load and supply are introduced at $t = 0.06\,\text{s}$ and $t = 0.08\,\text{s}$, respectively, in order to evaluate the robustness of the controllers. The load current increases as seen in Figs. 2 and 3 due to the occurrence of a load disturbance at $0.06\,\text{s}$. However, the SM controller is designed in such a way as to modify the duty cycle, in order to minimize the error generated because of the deviation of the output from its reference value and to maintain the desired output voltage in both cases

The input current frequency spectra displayed in Figs. 4 and 5 are obtained for the same operating state. It is observed that both PI and SM controllers offer more or less the same power quality, which is further substantiated through a THD (Total Harmonic Distortion) versus Power Factor graph shown in Fig. 6. The THD computed for output voltage at the same operating point, depicted in the bar diagram in Fig. 7 brings out the role of the SM controller.

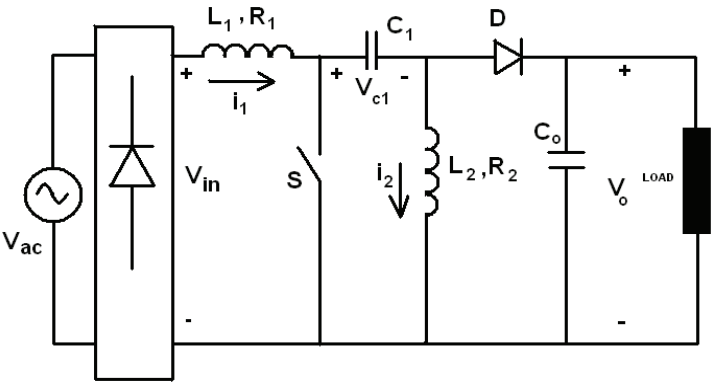

Fig. 1 – SEPIC *converter*.

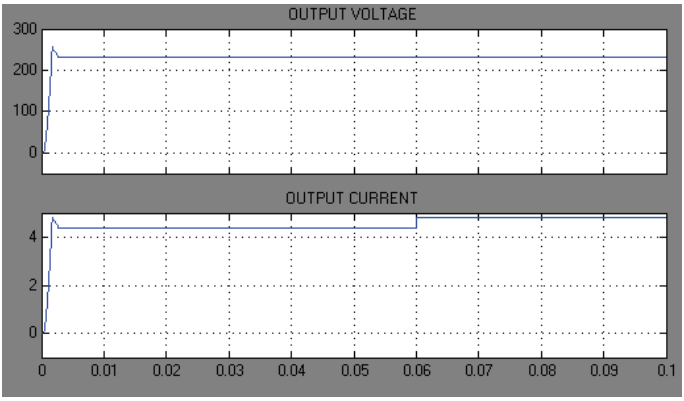

Fig. 2 – *Buck mode.*

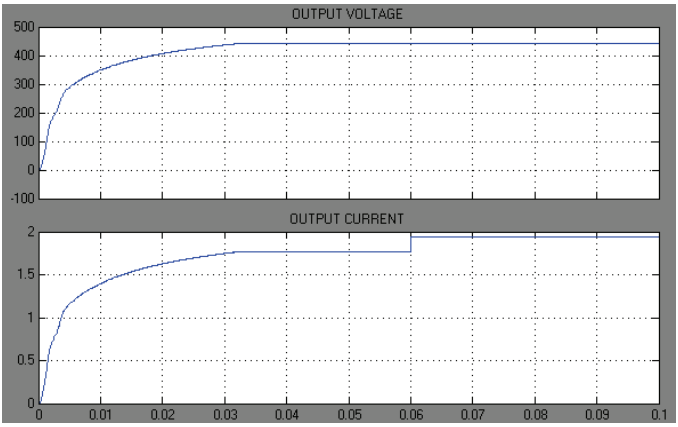

Fig. 3 – *Boost mode.*

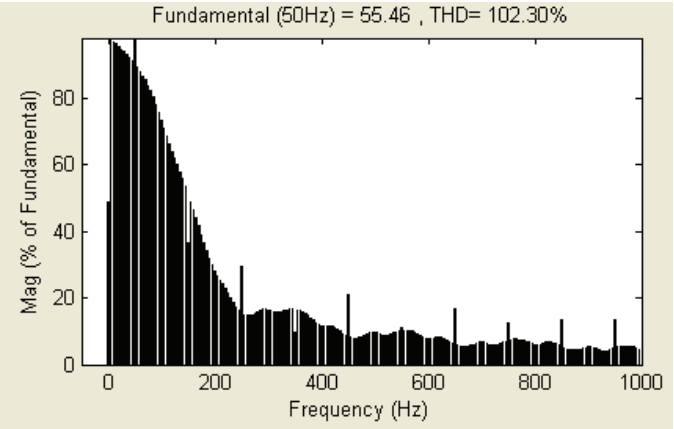

Fig. 4 – *Frequency spectrum of* PI *controller*.

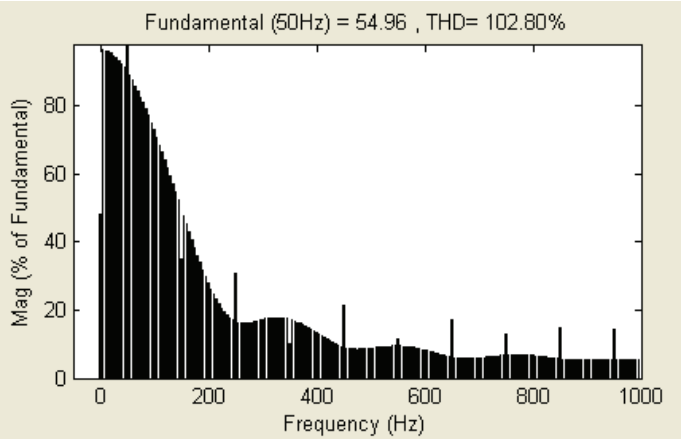

Fig. 5 – *Frequency spectrum of* SM *controller*.

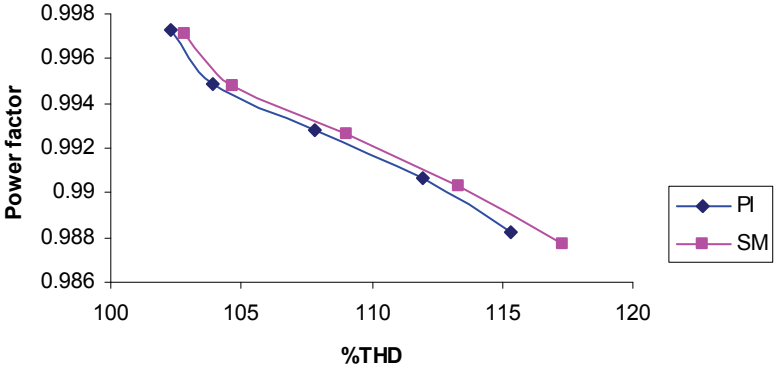

Fig. 6 – %THD *vs. Power factor*.

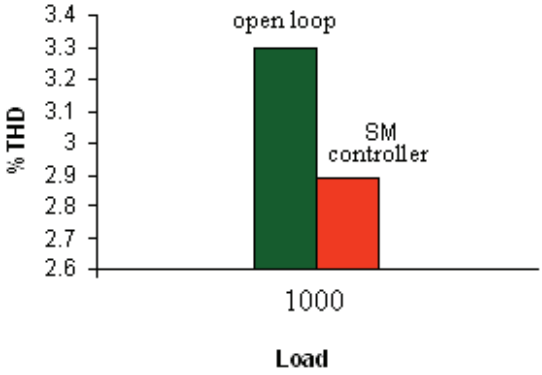

Fig. 7 – *Load vs.* %THD.

The SM controller, besides regulating the output voltage, reduces the wide distortion in the input current. It can be noticed that there is minimal overshoot during start-up while using the SM controller, thus highlighting the superiority of the SM controller. The conventional PI controller is seen to offer a second order response with a higher peak overshoot. However the SM controller is observed to give a first order response with no overshoot. It follows from **Table 1** that the time response specification of an SM controller is far better than that of a PI controller for a SEPIC.

Table 1
Time response of PI *and* SM *in buck mode*.

Load	% MP		Rise time [ms]		Peak time [ms]		Settling time [ms]	
	PI	SM	PI	SM	PI	SM	PI	SM
1000	86.74	4.07	1.660	1.667	3.100	1.735	18.00	2.80
2000	83.09	4.27	1.704	1.703	3.120	1.775	10.40	2.33
3000	86.66	3.94	1.725	1.725	3.220	1.793	8.56	2.13
4000	88.35	3.85	1.760	1.764	3.315	1.832	6.28	2.10
5000	91.01	3.97	1.780	1.785	3.400	1.856	4.92	2.08

6 Hardware Implementation

The prototype model shown in Fig. 8 is built for 5kW and tested for similar values of load powers. DSPIC is a single chip embedded controller that seamlessly integrates the control attributes of a microcontroller with the computation throughput capabilities of DSP in a single core. The DSPIC processor is programmed to function both as a PWM generator and an SM

controller. The algorithm is tailor-made to calculate the switching function for the SM controller, which in turn serves to alter the duty cycle of the SEPIC converter. The PWM pulses and the steady state output voltage waveform obtained from the prototype are displayed in Figs. 9 and 10 respectively.

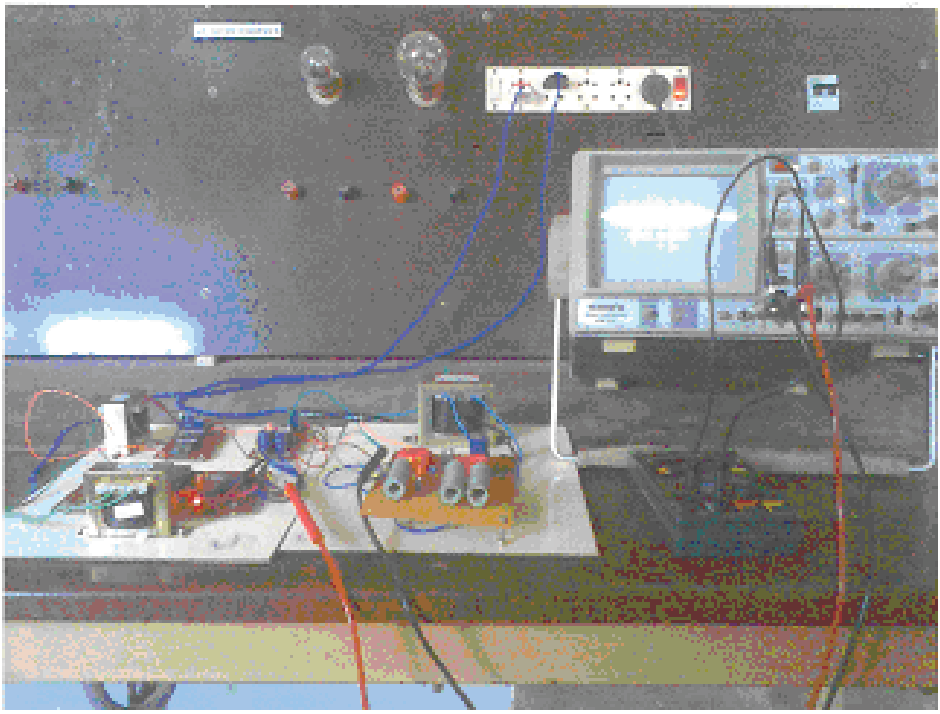

Fig. 8 – *Experimental setup*.

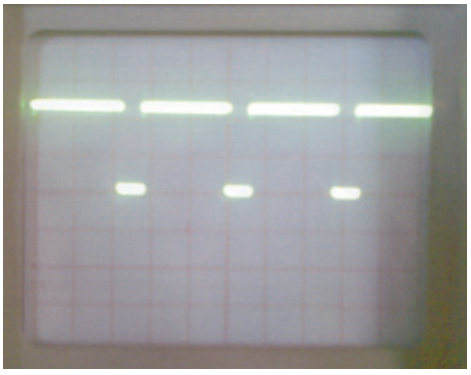

Fig. 9 – PWM *Pulse*.

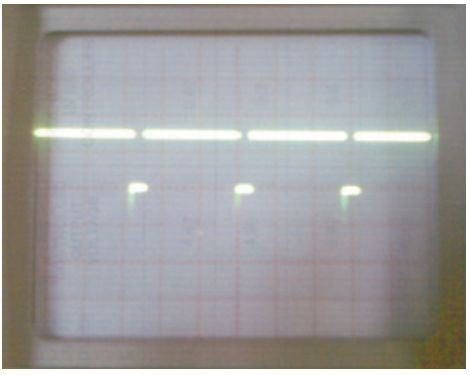

Fig. 10 – *Output Voltage*.

The experimental results obtained over a wide range of load variations seen in **Table 2** closely compare with the simulated performance. The entries in **Table 3** serve to highlight the regulating action of the SM controller.

Table 2
Comparison of simulation and hardware results.

Load [kW]	Load Current [A]	Output Voltage [V]		Input Power Factor	
		Hardware	Simulation	Hardware	Simulation
1000	4.4	228.9	229.3	0.99	0.9971
2000	8.8	229	229.7	0.99	0.9948
3000	13.2	229.2	229.5	0.99	0.9926
4000	17.6	229.3	229.8	0.99	0.9903
5000	22.0	229.1	229.6	0.98	0.9877

Table 3
Comparison of simulation and hardware results with load and source disturbances.

		Time [s]	V_L [V]	
			Before	After
(10%) Source disturbance	Simulation	0.08	230.4	230.3
	Hardware	0.08	230.1	230.5
(10%) Load disturbance	Simulation	0.06	230.2	229.9
	Hardware	0.06	230.5	229.2

7 Conclusion

A DSPIC processor has been programmed to generate the trigger pulses for the power switch in a SEPIC buck/boost converter and function as a PI/SM controller. The implementation of the designed control algorithm has been found to offer very good time response performance and acceptable power quality, in addition to regulating the output voltage. The results having demonstrated the suitability of the proposed approach for use in critical applications, will go a long way in enhancing the scope of such converters.

8 References

[1] K. Matsui, I. Yamamoto, T. Kishi, M. Hasegawa, H. Mori, F. Ueda: A Comparison of Various Buck-Boost Converters and their Application to PFC, IEEE Indust. Electronics Conf. IECON 02, 5-8 Nov. 2002, Vol. 1, pp. 30 – 36.

[2] R.B. Ridley: A New Continuous-time Model for Current-mode Control, IEEE Transaction on Power Electronics, Vol. 6 , No 2, April 1991, pp. 271 – 280.

[3] C-M. Lee, Y.S. Lai: Averaged Switch Modeling of DC/DC Converters using New Switch Network, Power Electronics and Drive System 2007, PEDS 07, 7th Int. Conf., 27-30 Nov. 2007, pp.1427 – 1430.

[4] W. Guo, P. Jain: Comparison between Boost and Buck-Boost Implemented PFC Inverter with Built in Soft Switching and Unified Controller, IEEE Power Electronics Specialists Conf. PESC 2001, pp. 472 – 477.

[5] C.K. Tse, M. di Bernado: Complex Behavior in Switching Power Converters, Proc. IEEE, Vol. 90, No. 5, May 2002, pp. 768 – 781.

[6] J.M. Kwon, W.Y. Choi, J.J. Lee, E.H. Kim, B.H. Kwon: Continuous Conduction Mode SEPIC Converter with Low Reverse-recovery Loss for Power Factor Correction, IEE Proc. Electric Power Application, Vol. 153, No. 5, September 2006, pp. 673 – 681.

[7] G. Spiazzi, P. Mattavelli: Design Criteria for Power Factor Pre Regulators Based on SEPIC and CUK Converters in Continuous Conduction Mode, IEEIAS, Denver, Oct.1994, pp. 1084 – 1089.

[8] A. Hren, P. Slibar: Full Order Dynamic Model of SEPIC Converter, IEEE ISIE 2005, 20-23 June 2005, Vol. 2, pp.553 – 558.

[9] K. Udhayakumar, P. Lakshmi, K. Boobal: Hybrid Posicast Controller for a DC – DC Buck Converter, Serbian Journal of Electrical Engineering, Vol. 5, No. 1, May 2008, pp. 121 – 138.

[10] J. Sebastian, J. Uceda, J.A. Cobos, J. Arau, F. Aldana: Improving Power Factor Correction in Distributed Power Supply Systems using PWM and ZCS-QR SEPIC Topologies, IEEE PESC 1991, pp. 780 – 791.

[11] W.M. Moussa: Modeling and Performance Evaluation of a DC/DC SEPIC Converter, Appl. Power Electronics Conf. and Expo. 1995, APEC ’95, Conf. Proc. 1995, 5-9 March 1995, Vol. 2, pp. 702 – 706.

[12] R.D. Middlebrook: Modeling Current-programmed Buck and Boost Regulators, IEEE Transaction on Power Electronics, Vol. 4, No. 1, Jan. 1989, pp. 36 – 52.

[13] O. Pop, G. Chindris, A. Grama, F. Hurgoi: Power Factor Correction Circuit with a New Modified SEPIC Converter, Electronics Technology: Concurrent Engineering in Electronic Packaging, 2001, 24th Int. Spring Seminar, 5-9 May 2001, pp. 117 – 120.

[14] W. Gu: Small Signal Modeling for Current Mode Controlled CUK and SEPIC Converters, Appl. Power Electronics Conf. and Expo. 2005, APEC 2005, Twentieth Annual IEEE, 6-10 March 2005, Vol. 2, pp. 906 – 910.

[15] M.B. Debbat, A. E1-Aroudi, R. Giral, L. Martienz-Salamero: Stability Analysis and Bifurcation of SEPIC DC-DC Converter using a Discrete-time Model, IEEE Int. Conf. Industry and Technol., ICIT ’02, Bangkok, Thailand, 11-14 Dec. 2002, Vol. 2, pp. 1055 – 1060.

[16] R. Tymerski, D. Li: State-space Models for Current Programmed Pulse width Modulated Converters, IEEE Transaction on Power Electronics, Vol. 8, No. 3, July 1993, pp. 271 – 278.