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More Stability and Robustness with the Multi-loop Control Solution for Dynamic Voltage Restorer (DVR)

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Abstract: This paper presents the application of dynamic voltage restorers (DVR) on power distribution systems for mitigation of voltage sags/swells at critical loads. DVR is one of the compensating types of custom power devices. An adequate modeling and simulation of DVR, including controls in MATLAB, based on forced-commutated voltage source converter (VSC), has been proved suitable for compensating the voltage sags/swells. In this paper, a double loop control method is proposed for the improvement of the stability of DVR during the load current variation. For the main loop (Outer Voltage Loop), we use a PI controller for the regulation of the filter condenser voltage. The second loop (Inner Current Loop) also uses a PI controller to control the disturbances current during load variation. Simulation results are presented to illustrate and understand the performances of DVR in the compensation of voltage sags/swell even with variation load condition.

Keywords: Custom power, Power quality, Voltage sags, Voltage swells, Current controller, Voltage controller, PWM, DVR.

1 Introduction

Modern power systems are complex networks where hundreds of generating stations and thousands of load centers are interconnected through long power transmission and distribution networks [1]. The main concern of consumers is the quality and reliability of power supplies at various load centers where they are located. Even though the power generation in most well-developed countries is fairly reliable, the quality of the supply is not entirely reliable. Power distribution systems, ideally, should provide their customers with an uninterrupted flow of energy at smooth sinusoidal voltage at the contracted magnitude level and frequency [2]. However, in practice, power systems, especially the distribution systems, have numerous nonlinear loads, which significantly affect the quality of power supplies. As a result of the

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nonlinear loads, the purity of the waveform of supplies is lost. This ends up producing many power-quality problems. Apart from nonlinear loads, some system events, both regular (e.g. condenser switching, motor starting) and iregular (e.g. faults) could also inflict power quality problems [3].

A power quality problem is defined as any problem manifested in voltage/current change or frequency deviations that result in failure or malfunctioning of a customer's equipment [3,4].

Power quality problems are associated with an enormous number of electromagnetic phenomena in power systems with broad ranges of time frames such as long duration variations, short duration variations and other disturbances. Short duration variations are mainly caused by either fault conditions or energising of heavy loads that require high starting currents. Different impedance-related electrical distances and types of grounding and connection of transformers between the faulted/load location and the node may induce a temporary loss of voltage or temporary voltage reduction (sag) or voltage rise (swell) at different nodes of the system [5].

Voltage sag is defined as a sudden plummet in voltage supply from 90% to 10% of nominally, followed by a recovery after a short period of time. A typical duration of the sag is l0 ms to 1 minute, according to the standard. Voltage sag can induce the production loss in automated processes since voltage sag can trip a motor or cause the controller to malfunction.

Voltage swell, on the other hand, is defined as a soar in voltage supply from 110% to 180% in rms voltage at the network fundamental frequency, its duration being from 10 ms to 1 minute.

Switching off a large inductive load or energising a large condenser bank is a typical system event that causes swells [1]. To compensate the voltage sag/swell in a power distribution system, appropriate devices need to be installed at adequate locations. These devices are typically installed at the point of common coupling (PCC) defined as the spot of change of the network ownership.

2 Dynamic Voltage Restorers

A DVR is a device that injects dynamically controlled voltage $V_{inj}(t)$ in series to the bus voltage by means of a transformer as depicted in Fig. 1. There are three single-phase transformers connected to a three phase converter with energy storage system and control circuit [5]. The amplitudes of the three injected phase voltages are controlled so as to eliminate any detrimental effects of a bus fault to the load voltage $V_L(t)$. This means that any differential voltage caused by transient disturbances in the ac feeder will be compensated by an

equivalent voltage generated by the converter and injected on the medium voltage level through the booster transformer.

The DVR operates independently of the type of fault or any event occuring in the system, provided that the whole system remains connected to the supply grid, i.e. the line breaker does not trip. For most practical cases, a more economical design can be achieved by only compensating the positive and negative sequence components of the voltage disturbance seen at the input of the DVR. This option is reasonable owing to typical distribution network configuration; the zero sequence part of a disturbance will not pass through the step down transformers owing to infinite impedance for this component.

For the most part DVR "does nothing" except monitoring the bus voltage, which means that it does not inject any voltage ($V_{inj}(t) = 0$) independent of the load current. Therefore, we recommend that the attention should be focused particularly on the losses of a DVR during normal operation. Two specific features addressing this loss issue have been implemented in its design, the transformer design including low impedance, and the semiconductor devices used for switching. An equivalent circuit diagram of the DVR and the principle of series injection for sag compensation are depicted in Fig. 2.

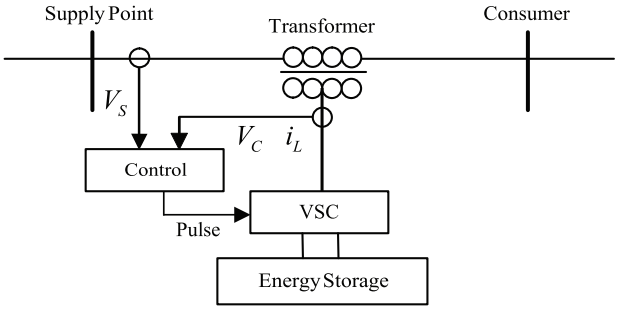

Fig. 1 – *Schematic diagram of DVR System.*

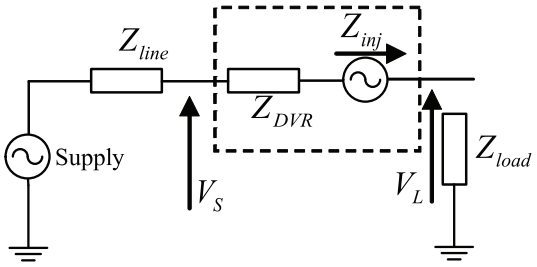

Fig. 2 – *Equivalent circuit of DVR.*

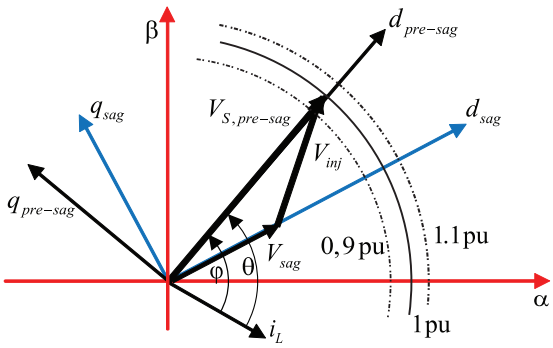

Fig. 3 – *Compensation strategy of DVR for voltage sags.*

Mathematically expressed, the injection satisfies:

$$V_L(t) = V_S(t) + V_{inj}(t), \tag{1}$$

where $V_L(t)$ is the load voltage, $V_S(t)$ is sagged supply voltage and $V_{inj}(t)$ is the voltage injected by the mitigation device as shown in Fig. 3. Under nominal voltage conditions, the load power on each phase is given by (2):

$$S_L = V_L I_L^* = P_L - \mathrm{j}Q_L, \tag{2}$$

where I_L is the load current, and P_L, and Q_L are the active and reactive power taken by the load respectively during a sag/swell. When the mitigation device is active and restores the voltages back to normal, the following applies to each phase:

$$S_L = P_L - \mathrm{j}Q_L = (P_S - \mathrm{j}Q_S) + (P_{inj} - \mathrm{j}Q_{inj}), \tag{3}$$

where sag subscript refers to the sagged supply quantities. The inject subscript refers to quantities injected by the mitigation device.

3 Control Strategy

For the identification of disturbance, we use the Park transformation technique (*dq*-frame) [2-4].

This work is primarily focused on closed-loop PWM control scheme (Fig. 4). The closed-loop control introduced in this paper is made up of an inner current loop and an outer voltage loop to better satisfy different linear or non-linear load disturbance. System level simulations of the whole inverter and control system will be performed based on MATLAB-Simulink. Proportional-plus-integral (PI) controller will be used in this dual-loop control system to regulate output voltage of the PWM inverter.

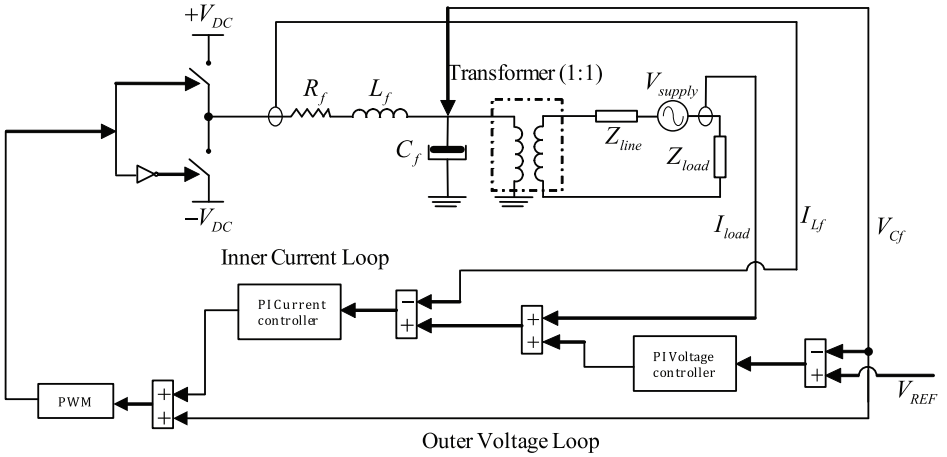

Fig. 4 – *Dual-loop control scheme for single-phase PWM inverter.*

The current and voltage dual-loop control system for a single-phase PWM inverter can effectively reduce the output voltage distortion and achieve fast dynamic response [7]. In this control scheme output voltage V_{Cf} and inductor current I_{Lf} will form an outer loop and an inner loop each governed by a PI controller. In additional, load current I_{load} and the output voltage V_{Cf} will act as feedback compensation for the reduction of output disturbance even under rough load conditions. The reference input will give the desired output voltage as a control reference.

To determine K_P and K_I values of both regulators, we study every loop independent of each other. Fig. 5 shows the control loop block diagram, where all the components are represented by their respective transfer functions or gains. In particular, the controller block is represented by the typical proportional integral regulator structure, whose parameters K_P and K_I will be determined in the following. The output of the regulator represents the modulating signal that drives the pulse width modulator. This has been modeled as the cascade combination of two separate blocks: the first one is the modulator static gain, and the second is actually a first-order Pade approximation of its delay, considered equal to a half of the duration of the modulation period.

Considering the inverter and load models, we see that they based on the analysis which is presented as follows. Finally, to fully replicate a typical implementation, a transducer gain is taken into account. Additional filters, normally adopted to clean the transducer signal from residual switching noise, are not taken into account, in favor of a more essential presentation. Their transfer functions can be easily cascaded to the transducer block gain if needed.

3.1 Inner current loop and design of the PI controller

At first, we want to determine the open loop gain for the block diagram of Fig. 5. This is given by the cascade connection of all blocks. We find

$$G_{OL}(t)=\left(K_P+\frac{K_I}{s}\right)\frac{2V_{DC}}{C_{PK}}\frac{1-s\frac{T_S}{4}}{1+s\frac{T_S}{4}}\frac{G_{TI}}{R_f}\frac{1}{1+s\frac{L_f}{R_f}}. \tag{4}$$

The regulator design is typically driven by specifications concerning the required closed loop speed of response or, equivalently, the maximum allowed tracking error with respect to the reference signal. These specifications can be turned into equivalent specifications for the closed loop bandwidth and phase margin. To give an example, we suppose that, for our current controller, a closed loop bandwidth, f_{CL}, equal to about one sixth of the switching frequency f_S is required, to be achieved with, at least, a 60° phase margin, *phm*.

We therefore have to determine the parameters K_P and K_I so as to guarantee the compliance to these requirements.

To rapidly get an estimation of the searched values, we suppose that we can approximate the open loop gain at the crossover angular frequency, i.e. at $\omega=\omega_{CL}=2\pi f_{CL}$ with the following expression:

$$G_{OL}(\mathrm{j}\omega_{CL})\cong K_P\frac{2V_{DC}}{C_{PK}}\frac{1-\mathrm{j}\omega_{CL}\frac{T_S}{4}}{1+\mathrm{j}\omega_{CL}\frac{T_S}{4}}\frac{G_{TI}}{R_f}\frac{1}{1+\mathrm{j}\omega_{CL}\frac{L_f}{R_f}}. \tag{5}$$

This, in principle, will be a good approximation as long as $K_I << \omega_{CL}K_P$ (to be verified later). Imposing now the magnitude of (5) to be equal to one at the desired crossover frequency, we get

$$K_P=\frac{C_{PK}}{2V_{DC}}\frac{R_f}{G_{TI}}\sqrt{1+\left(\omega_{CL}\frac{L_f}{R_f}\right)^2}. \tag{6}$$

The parameter K_I can then be calculated considering the open loop phase margin and imposing that to be equal to *phm*. We find from (4)

$$-180^0 + phm = -90^0 - 2\tan^{-1}\left(\omega_{CL}\frac{T_S}{4}\right) - \tan^{-1}\left(\omega_{CL}\frac{L_f}{R_f}\right) + \tan^{-1}\left(\omega_{CL}\frac{K_P}{K_I}\right), \quad (7)$$

which yields

$$K_I = \frac{\omega_{CL}K_P}{\tan\left(-90^0 + phm + 2\tan^{-1}\left(\omega_{CL}\frac{T_S}{4}\right) + \tan^{-1}\left(\omega_{CL}\frac{L_f}{R_f}\right)\right)}. \quad (8)$$

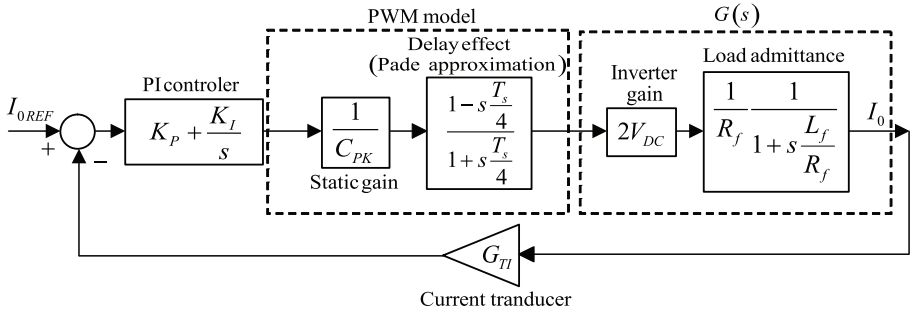

Fig. 5– *Control loop block diagram.*

Note that (8) is exact; only the K_P value is obtained through an approximation. Considering the parameters listed in **Table 1** and $\omega_{CL} = \frac{2\pi f_S}{6} \cong 52.4\,\text{krads}^{-1}$, we can immediately find the following values:

$K_P = 6.284$ and $K_I = 1.802 \cdot 10^4$ rads^{-1}.

It is easy to verify that the condition $K_I << \omega_{CL}K_P$ is reasonably met by this solution.

This occurs in vast majority of practical cases, so that (6) and (8) can be very often directly used.

3.2 Outer voltage loop and design of the PI controller

The voltage PI controller gains can be determined once the desired loop bandwidth, f_{CL}, is specified. For a DVR application, in order to achieve a satisfactory control of the voltage waveform in the presence of distorting loads. While this is easy to obtain when the switching frequency is relatively high, as it is in our case, and the current controller is a fast one, like the one we are considering here, in the opposite case, i.e., when a low switching frequency

application is considered or when the internal control loop is relatively slow, it may not be too easy to achieve the desired values.

However, once f_{CL} is known, we can consider the open loop gain expression and force its magnitude to be equal to one at the desired crossover frequency. From Fig. 6 the open loop gain is found to be:

$$G_{OL-V} = \frac{G_{TV}}{G_{TI}} \frac{1 - sT_S}{1 + sT_S} \frac{1}{sC_f \left(K_P + \frac{K_I}{s} \right)}. \tag{9}$$

It is worth noting that, differently from the current controller case, no delay effect related to the holder has been taken into account. This is possible because the internal current control loop has been designed to compensate for that. Therefore, the only dynamic delay the voltage controller has to compensate is that of the current controller.

Given (9), the first condition we need to satisfy by suitably choosing K_P and K_I is as follows:

$$\frac{G_{TV}}{G_{TI}} \frac{\sqrt{K_I^2 \left(\omega_{CL} K_P \right)^2}}{\omega_{CL}^2 C_f} = 1. \tag{10}$$

where, as usual, $\omega_{CL} = 2\pi f_{CL}$.

The second constraint we can impose is requiring a minimum phase margin, *phm*, for the loop gain at the crossover frequency. In order to get a reasonable damping of the dynamic response, this can be set equal to 60°. Consequently, we find the following additional condition:

$$-180^0 + phm = -180^0 - 2\tan^{-1}\left(\omega_{CL} T_S \right) + \tan^{-1}\left(\omega_{CL} \frac{K_P}{K_I} \right). \tag{11}$$

The solution of the system of equations (10) and (11), considering the parameter values listed in **Table 1** and imposing $f_{CL} = 1800\text{Hz}$ provides us with the following values for the PI gains: $K_P = 3.81$ and $K_I = 3.42 \cdot 10^3$ rads^{-1}.

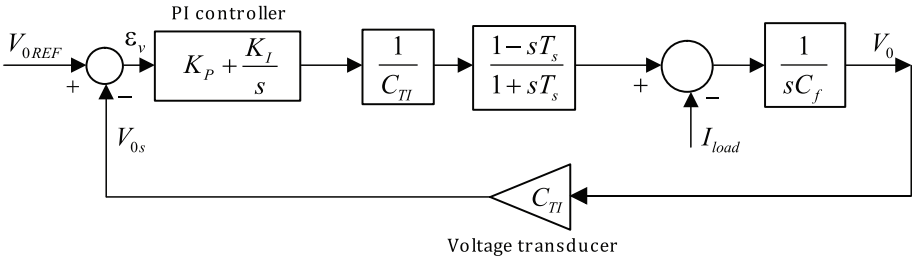

Fig. 6 – *Control loop block diagram.*

Table 1
Parameters.

Filter inductance	$L_f = 1.5\,\text{mH}$
Filter resistance	$R_f = 0.002\,\Omega$
Filter condenser	$C_f = 68\,\mu\text{F}$
Phase supply voltage	$V_S = 110\,\text{Vrms}$
DC link voltage	$V_{DC} = 250\,\text{V}$
Supply frequency	$60\,\text{Hz}$
PWM carrier peak	$C_{PK} = 4\,\text{V}$
Switching frequency	$f_S = 50\,\text{kHz}$
Current transducer gain	$G_{TI} = 0.1\,\text{VA}^{-1}$
Voltage transducer gain	$G_{TV} = 0.02\,\text{VV}^{-1}$
Transformer rapport	1:1
Phase margin	$phm = 60°$

4 Simulation Results

In order to understand the performance of the DVR along with control, a simple power supply network is presented in Fig. 7. A DVR is connected to the system through a series transformer with a rapport transformation equal to 1:1. The DVR is based on three phase voltage PWM inverter with LC output filter to remove high frequency voltage components. An *R-L* load ($R = 10\Omega$, $L = 10^{-6}\,\text{H}$) is considered.

First, a case of symmetrical sag is simulated by connecting and disconnecting a three-phase reactance to the busbar. The results are shown in Fig. 8a 30% voltage sag is initiated at 0.05s and it is kept until 0.15s. Figs. 9b and 9c show the voltage components injected by the DVR and compensated load voltage, respectively. As a result of DVR use, the load voltage is kept at 110 Vrms.

In order to show the performance of the DVR under critical conditions, a phase (a) of supply voltage outage at 0.052 s is simulated. The DVR is immediately compensating the voltage phase absence. The results are shown in Fig. 9.

It can be seen, from the results, that the DVR is able to produce the required compensating voltage components for different phases rapidly and help to maintain a balanced and constant load voltage at 110 Vrms.

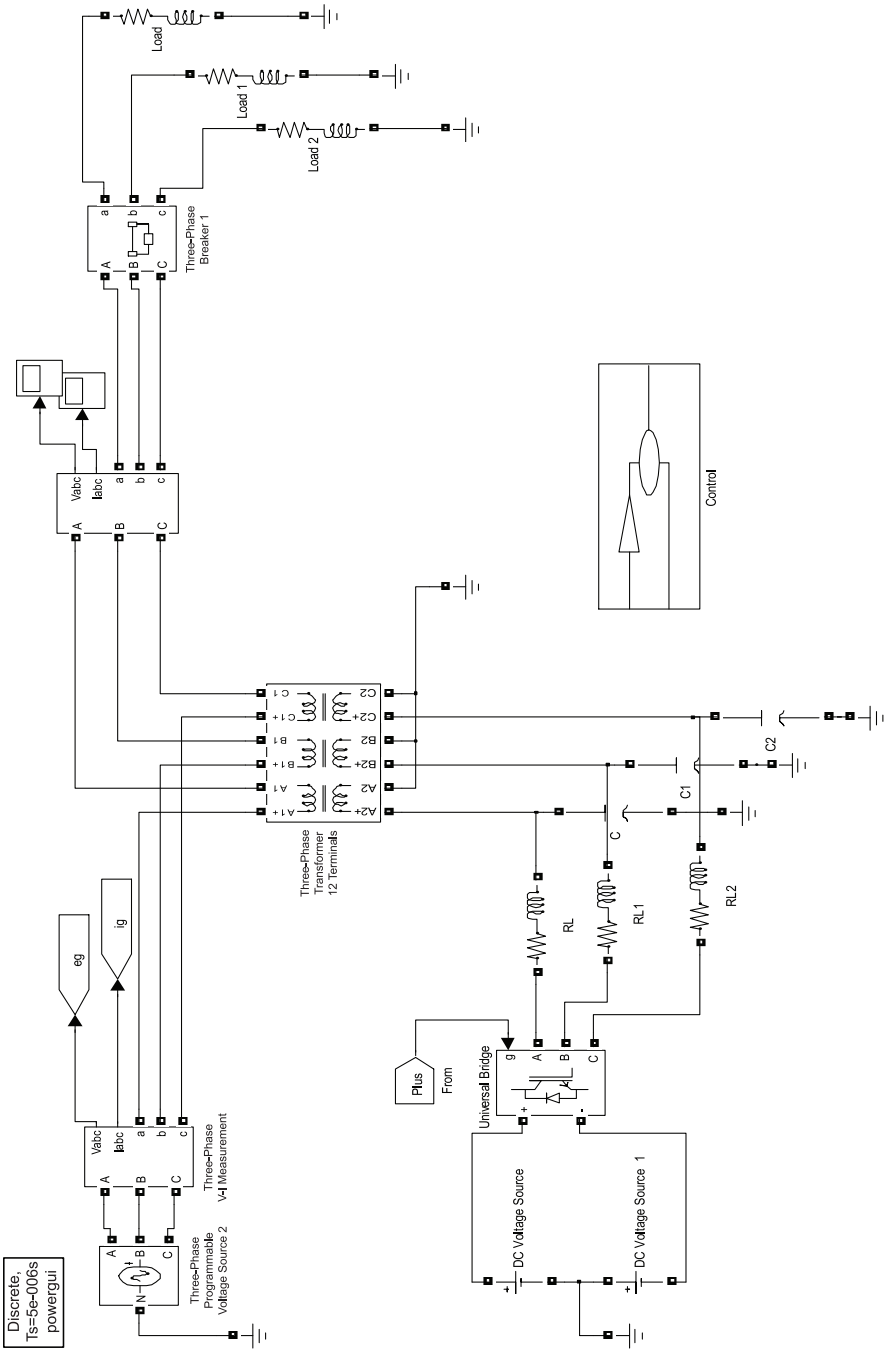

Fig. 7 – *DVR coupling in power system.*

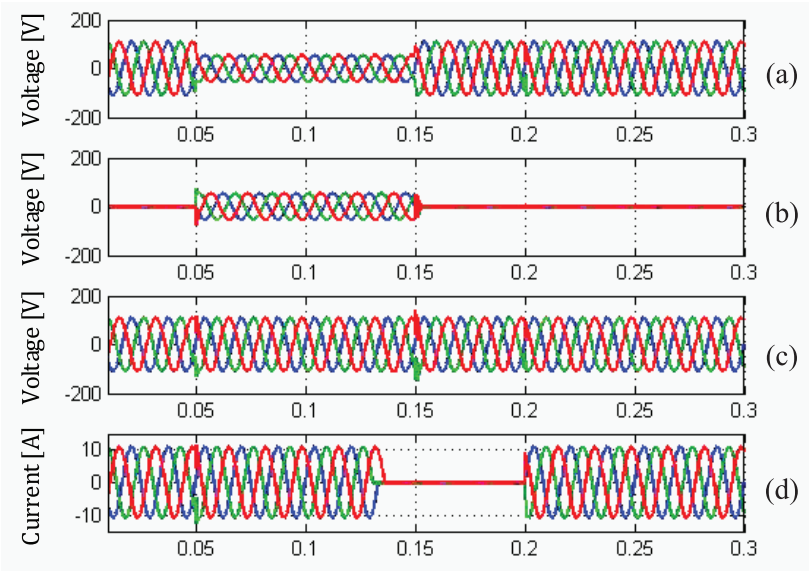

Fig. 8 – *Simulation result of DVR response to a balanced voltage sag with connection and disconnection load: (a) supply voltage, (b) DVR injected voltage, (c) load voltage, (d) load current.*

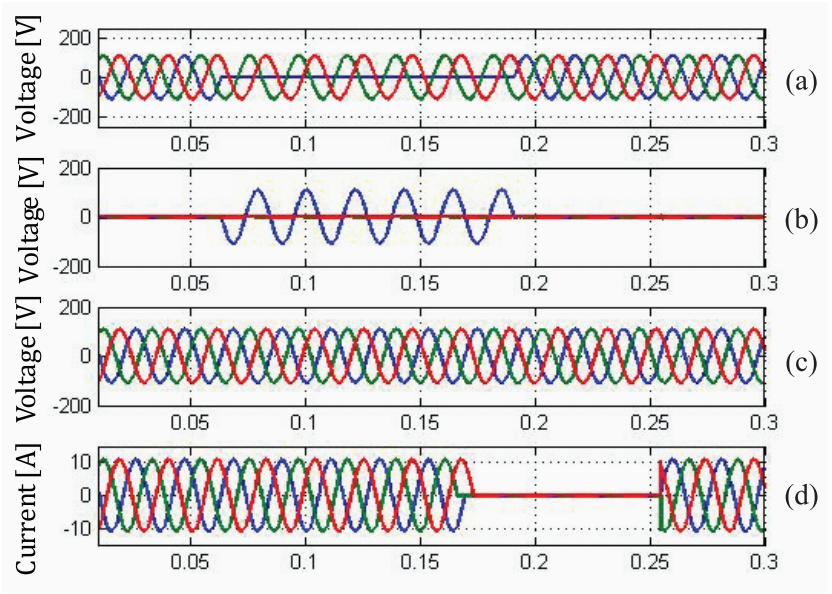

Fig. 9 – *Simulation result of DVR response to a phase voltage outage with connection and disconnection load:* a) *supply voltage,* b) *DVR injected voltage,* c) *load voltage,* d) *load current.*

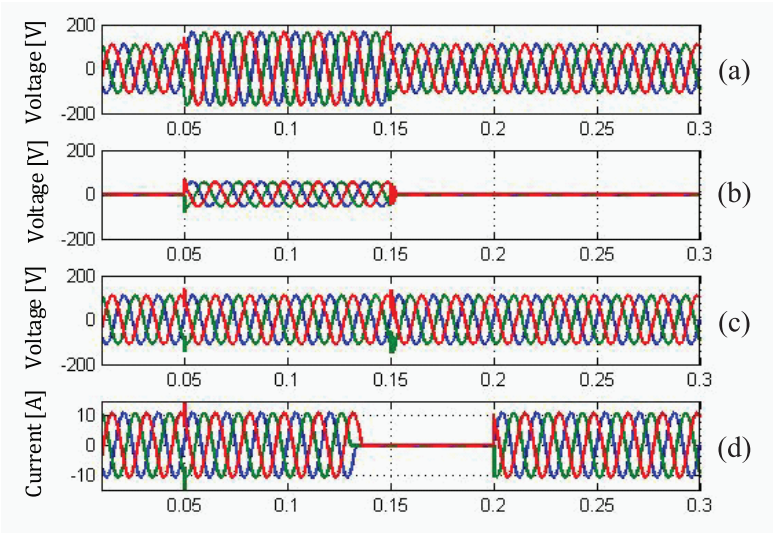

Fig. 10 – *Simulation result of DVR response to balance voltage swill with connection and disconnection load: a) supply voltage, b) DVR injected voltage, c) load voltage, d) load current.*

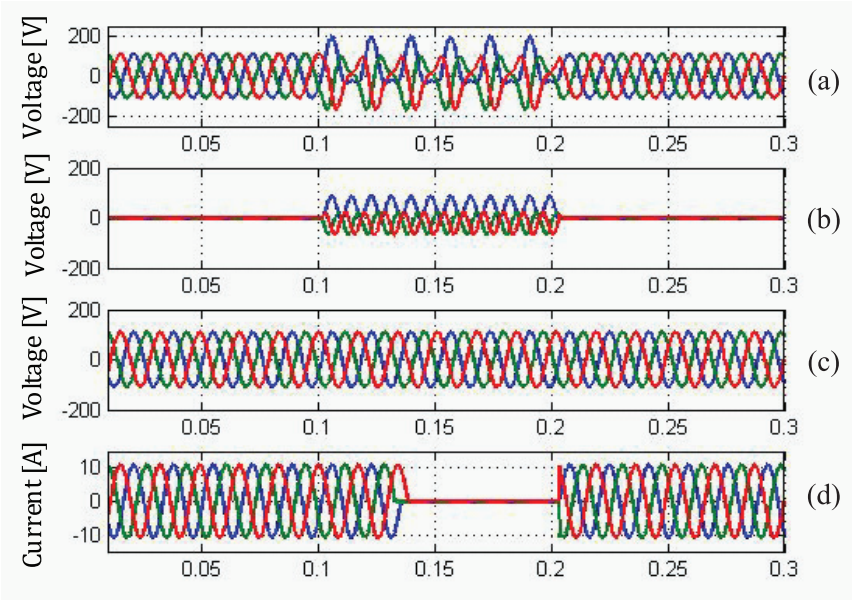

Fig. 11 – *Simulation result of DVR response to unbalance voltage deformation with connection and disconnection load: a) supply voltage, b) DVR injected voltage, c) load voltage, d) load current.*

Next, the performance of DVR for a voltage swell condition is investigated. The results are shown in Fig. 10a. The voltage amplitude is increased about l50% of nominal voltage. The injected voltage that is produced by DVR in order to correct the load voltage and this former are shown in Figs. 10b and 10c, respectively. As can be seen from the results, the load voltage is kept at the nominal value. Similar to the case of voltage sag, the DVR reacts quickly to inject the appropriate voltage component to correct the supply voltage.

The performance of the DVR with an unbalanced voltage deformation is shown in Fig. 11. The compensating voltage injected by the DVR is shown in Fig. 11b and the load voltage is given in Fig. 11c. Notice the constant and balanced voltage across the load.

In this part, we tested the DVR robustness in the critical condition due to the load current prompt variations. This robustness is tested using a double-loop control technique that ensures the control at the same time of voltage and DVR injected current. The first loop named Outer Voltage Loop, controls through a PI regulator the voltage across of the condenser C_f .

The second loop, named Inner Current Loop, controls through also a PI regulator the current flowing in the inductance L_f with load current prompt variation.

In all the above Figs. 8d, 9d, 10d and 11d the load current variation (disconnection and connection of the load) does not influence the stability of compensating injected DVR voltage.

5 Conclusion

In this paper, performance of a DVR in mitigating voltage sags/swells is demonstrated with the help of MATLAB. The DVR handles both balanced and unbalanced situations without any difficulties and injects the appropriate voltage component to correct any anomaly in the supply voltage to keep the load voltage balanced and constant at the nominal value. In the case of voltage sag, which is a condition of a temporary reduction in supply voltage, the DVR injects an equal positive voltage component in all three phases, which are in phase with the supply voltage to correct it. On the other hand, for a voltage swell case, which is a condition of a temporary increase in supply voltage, the DVR injects an equal negative voltage in all three phases, which are anti-phase with the supply voltage. For unbalanced conditions, the DVR injects an appropriate unbalanced three-phase voltage components positive or negative depending on whether the condition is an unbalanced voltage sag or unbalanced voltage swell.

The proposed control solution is the most important issue of this paper. The current and voltage dual-loop control system for a PWM inverter can effectively reduce output voltage distortion and achieve fast dynamic response.

6 References

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