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The Modeling and the Analysis of Control Logic for a Digital PWM Controller Based on a Nano Electronic Single Electron Transistor

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Abstract: This paper describes the modelling and the analysis of control logic for a Nano-Device- based PWM controller. A comprehensive simple SPICE schematic model for Single Electron transistor has been proposed. The operation of basic Single Electron Transistor logic gates and SET flip flops were successfully designed and their performances analyzed. The proposed design for realizing the logic gates and flip-flops is used in constructing the PWM controller utilized for switching the buck converter circuit. The output of the converter circuit is compared with reference voltage, and when the error voltage and the reference are matched the latch is reset so as to generate the PWM signal. Due to the simplicity and accuracy of the compact model, the simulation time and speed are much faster, which makes it potentially applicable in large-scale circuit simulation. This study confirms that the SET-based PWM controller is small in size, consumes ultra low power and operates at high speeds without compromising any performance. In addition, these devices are capable of measuring charges of extremely high sensitivity.

Keywords: Pulse Width Modulation, CMOS, Single Electron Transistor, Converter.

1 Introduction

Advances in integrated circuit technology have been mostly based on CMOS [1] circuit technology operating on the basis of binary logic. However, major problems in present day LSI technology, such as increased power consumption, interconnect delay, limited integration density and device scaling limits cannot be addressed simply by improving the conventional CMOS technology. An advanced device/circuit technology that achieves higher functionality with fewer hardware components will be desirable in the next generation low-power system on chip (SOC) architecture. Emerging nano devices provide achieving high functional density and extremely low power

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operation in principle. Nanotechnology has been a field of growing interest during the past decades, which offers the promise of ultra low power and ultra high integration density. It encompasses the creation and utilization of materials, devices and systems at the levels of atoms and molecules. Nanotechnology is being increasingly used in various disciplines and hence it is a highly interdisciplinary field. It is being used in semiconductor electronics, sensor applications, actuator applications, environmental applications and biomedical applications [2]. In addition, nano devices switching speed will be comparatively higher than the conventional devices. Nano electronics is a technology wherein a few electrons are sufficient to define a logic state. Instead of working with current and at voltage levels defined by millions of electrons in today's CMOS technology, one can realize the limit of calculating with few electrons. Single Electron transistor is one of the Nano Electronic devices which can be easily operated at room temperature hence the device has been considered when realizing the digital logic system. Advanced single electron devices, especially SET-based logic gates, are modelled according to the physical device of the model. The conventional CMOS is replaced by the SET in PWM controller circuits. The control is implemented in the programmable compensator which computes new duty ratio pulse to switch the converter circuits.

2 Single Electron Transistor

SET is the most fundamental of various single electron devices. It is capable of measuring charges with extremely high sensitivity. The functionality of the SET is analogous to that of a conventional transistor [3]. A normal transistor has three contacts, named source, the drain and the gate. The current between the source and the drain contacts can be controlled through the gate contact, making it possible to use the transistor as an amplifier; a small change in the gate signal induces considerable change in the source-drain current. An SET comprises a device similar to that of Coulomb blockade and is provided with an additional metallic connection. As compared with standard transistor, the contacts are named the source, the drain and the gate, as shown in Fig.1. The SET must have a small conductive island to exploit the coulomb blockade for manipulating electrons by means of one-by-one transfer. The gate is coupled capacitive to the metallic island, therefore changing the charge on the gate shifts the positions of electron energy levels of the island. Since the current through the island is dependent on these levels, changing the gate charge can effectively control the source-drain current.

A very simple SPICE schematic model for Single Electron transistor has been designed and used in this work. The SET equivalent circuit using switch model is shown in Fig. 2. It consists of two diodes and two bidirectional

switches. When no gate voltage is applied the switch is turned off and no conduction occurs. This period is called coulomb blockade. When gate voltage is applied the switch is turned on whereby the current conduction from drain to source occurs. The SET I-V characteristics are shown in Fig. 3. At the beginning, the curve is zero indicating coulomb blockade, whereas when the gate voltage is higher than 20mv, the coulomb blockade removed and the switch is turned on, which makes the curve to increases linearly. Here the coulomb blockade value is 20mv, and the characteristics obtained are similar to real time model [4].

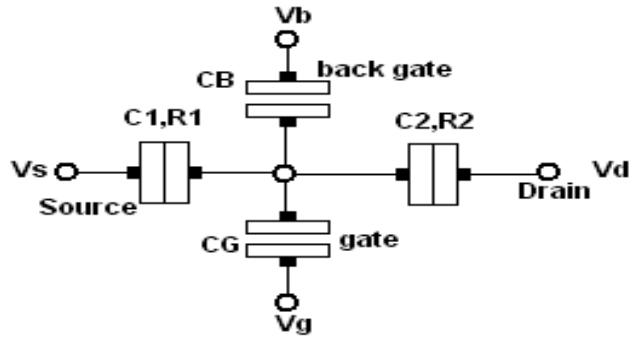

Fig. 1 – SET *Symbol.*

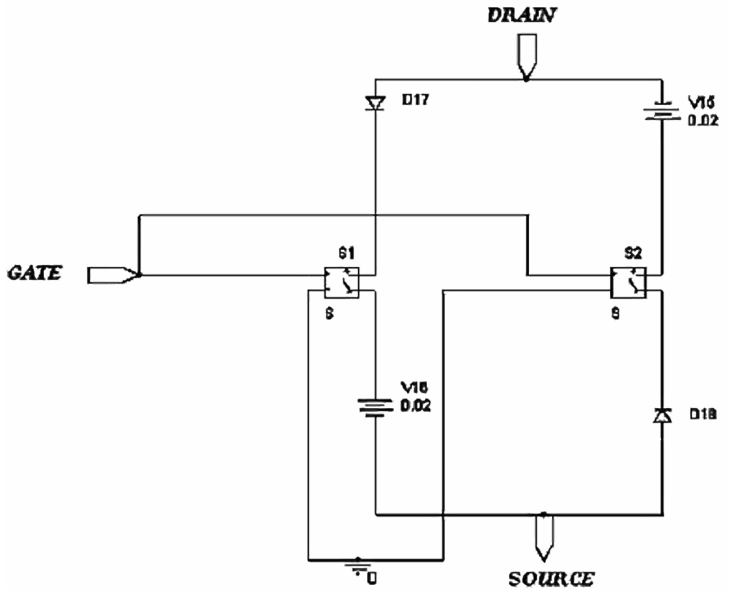

Fig. 2 – SET *Equivalent Circuit-Model.*

A straightforward electrostatic calculation shows that the voltage of the island as a function of the number of electrons on the island is

$$V(n) = \left(-ne + Q_0 + C_1 V + C_2 V_2 + C_{g1} V_{g1} + C_{g2} V_{g2}\right) / C_\Sigma \tag{1}$$

where n is the number of electrons on the island, e is the positive elementary charge, and C_Σ stands for the total capacitance of the island,

$$C_\Sigma = C_1 + C_2 + C_{g1} + C_{g2} + C_0 .$$

The energy required to move an infinitesimally small charge $\mathrm{d}q$ from ground at a potential $V = 0$ to the island is $V\,\mathrm{d}q$. As soon as charge is added to the island, the voltage of the island changes [5]. The energy needed to take a whole electron from ground and put it on the island is as follows:

$$\int_0^{-e} V\,\mathrm{d}q = -eV(n) + e^2/2C_\Sigma , \tag{2}$$

n being the number of electrons on the island before the final electron is added. The term $E_c = e^2/2C_\Sigma$ is called the charging energy which sets the energy scale for single-electron effects. This simple model has been used to realise the various modules of control strategy adopted here for PWM signal generation.

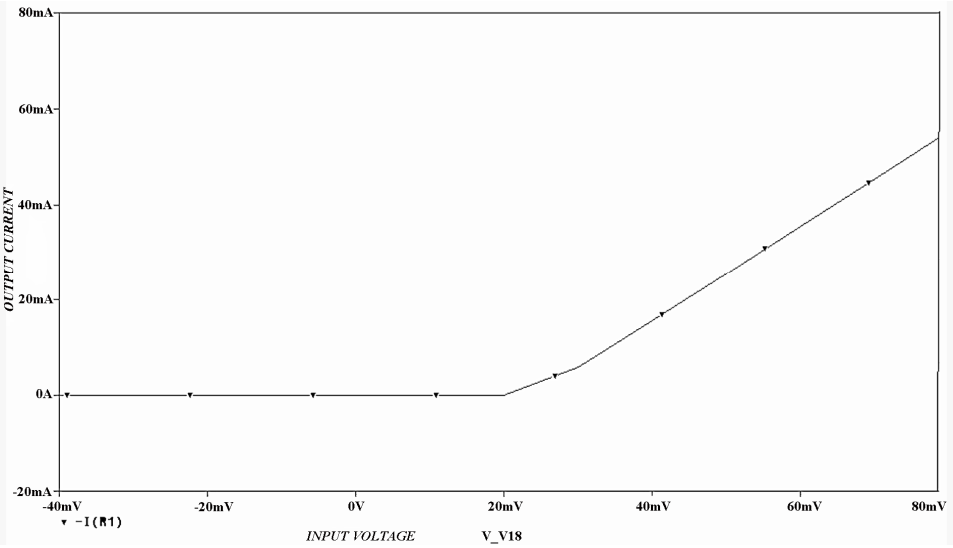

Fig. 3 – SET I-V *characteristics–Model* 3.

3 Basic Logic Gates and Flip Flops using SET

The family of logic gates and flip-flops that use SETs for realizing the control circuits have been discussed in this section. Since the gates and flip-flops are the primary requirement for analyzing control circuits, we shall present a detailed study of these circuits [6].

The SET inverter is presented in Fig. 4. When combining two complementary-biased SET transistors in a single circuit, we arrive at the SET inverter structure [7]. The upper SET transistor behaves similarly to a p-type transistor, while the lower transistor operates similarly to an n-type transistor. Output switching (from 0 to 1) is accomplished either by transporting electrons (commonly over 100) from the output node n2 to the top supply voltage terminal V_s or (from 1 to 0) by transporting electrons from the bottom ground terminal to the output node n2. Given the SET transistors can be biased in such manner that they behave similarly to p or n transistors, we can convert existing CMOS cell libraries to their SET equivalents [8].

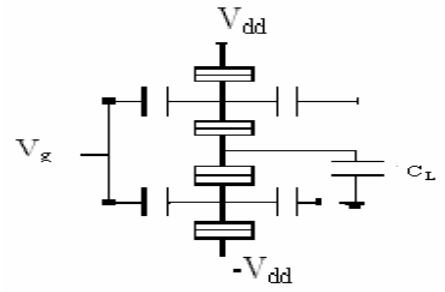

Fig. 4 – *An inverter*

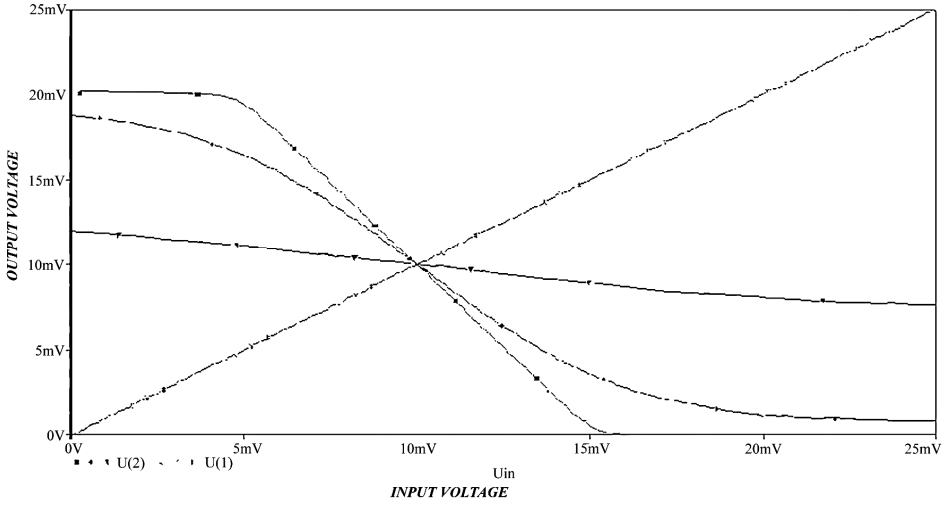

Fig. 5 – *Inverter Output Response.*

The Fig. 5 confirms the exact functioning of an inverter.

The implementation of NOR gate and its response is presented in Figs. 6 and 7, respectively. The main advantage of the approach is the re-utilization of existing knowledge and tools. Once a family of Boolean logic gates has been developed in a novel technology such as the SET, existing gate level designs of (larger) components [9], such as adders, multipliers, etc., can be realized in a straightforward manner. Equally important, existing design tools can be ported at very little cost and effort. The main disadvantage of this approach is induced by the fact that usually a technology is most likely not utilized to its full potential when it is mold to mimic an existing technology.

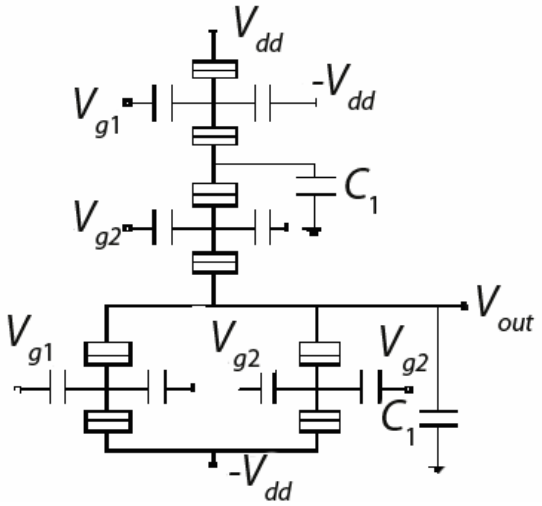

Fig. 6 – SET-NOR *Gate*

Focusing on SET [10], the CMOS like design style has the following disadvantages. First, the designs only operate correctly when the current though an "open" transistor consists of a large number of electrons. Given that electron tunneling is a sequential process, this is obviously a far slower process then the transport of only one electron through the same junction. Second, the "closed" transistor is not completely closed, resulting in a static current and a dramatic increase in power consumption. The implementation of NAND gate is shown in Fig. 8. Arranging the SETs in the structure as shown in Fig. 9 provides realizing of NAND gate logic. The implementation of AND gate and its response are shown in Figs. 10 and 12. Placing a SET inverter at the output terminal of the NAND gate obtains the AND gate realization. Placing an inverter at the output terminal of NOR gate provides the OR gate realization and consequently its output response (Figs. 11 and 13). The Figs. 14a and b shows the implementation of D flip-flop. When the clock input is high the output follows

the D input. Thus these SET-based gates and flip flops are replaced in conventional CMOS circuit for realizing PWM controller.

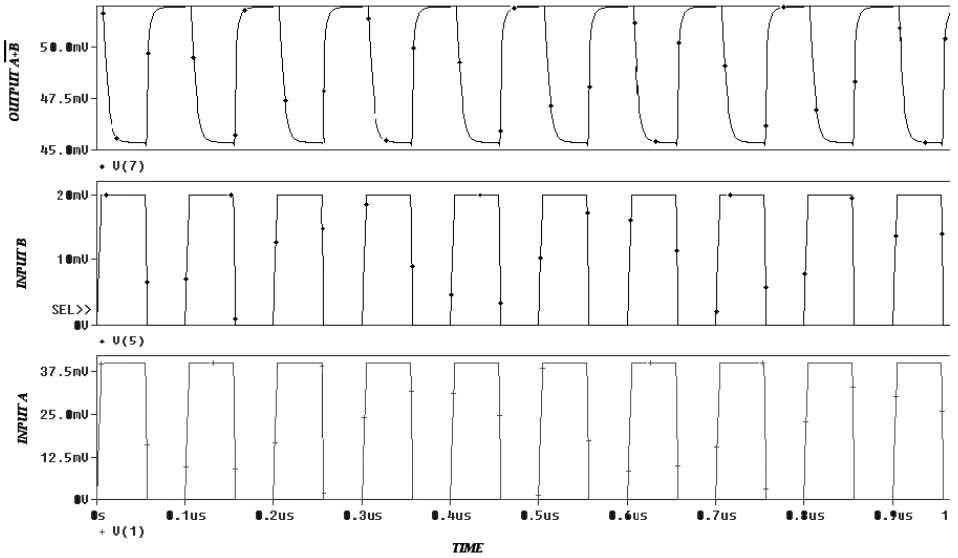

Fig. 7 – NOR *Gate input and Output Response.*

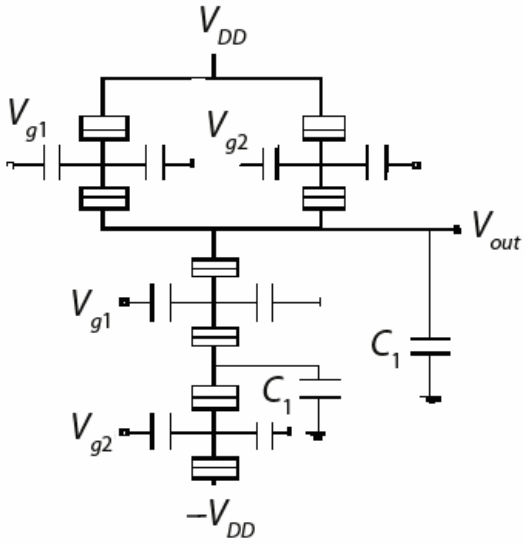

Fig. 8 – SET-NAND *Gate.*

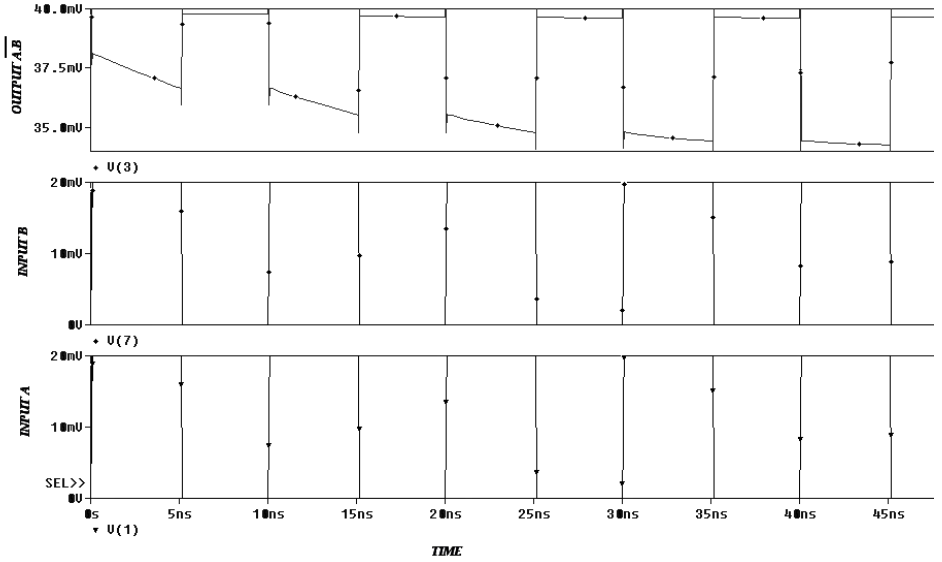

Fig. 9 – NAND *Gate input and output Response*.

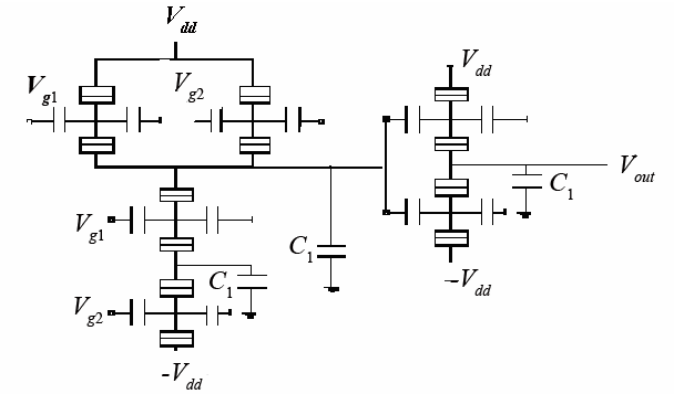

Fig. 10 – SET- AND *Gate.*

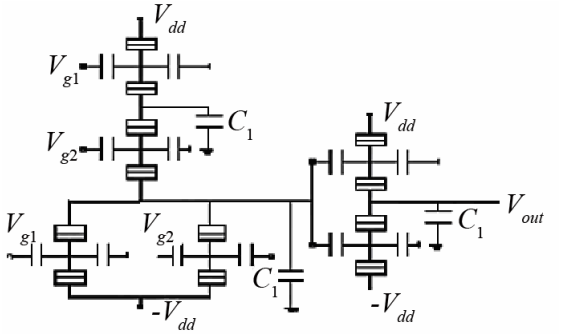

Fig. 11 – SET-OR *Gate.*

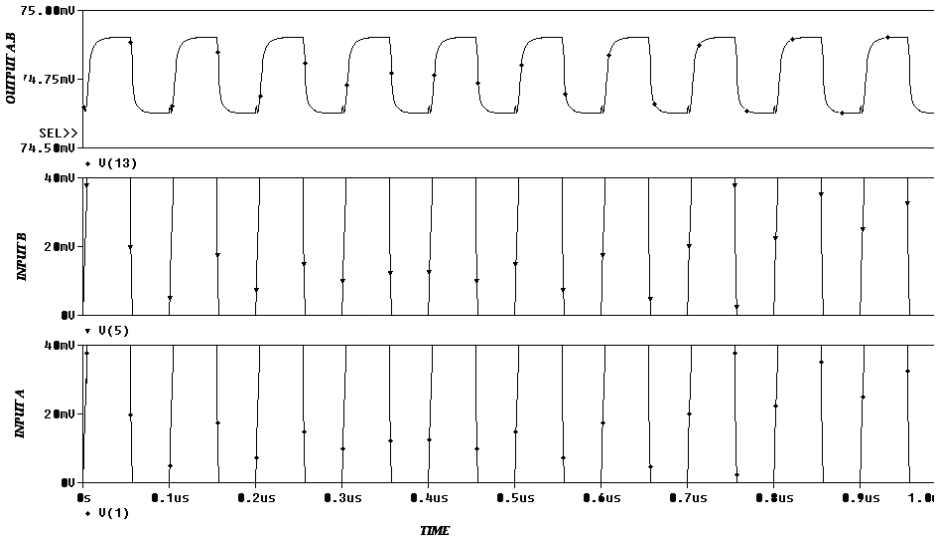

Fig. 12 – AND *Gate input and output Response.*

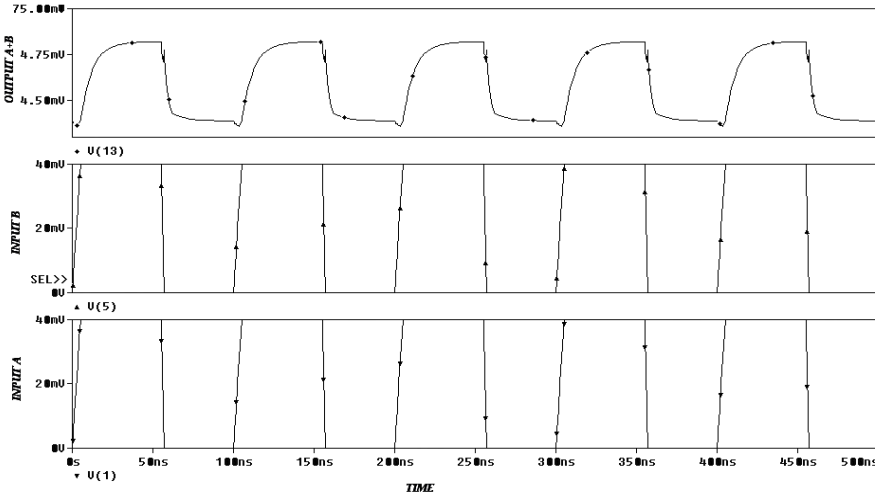

Fig. 13 – OR *Gate input and output Response.*

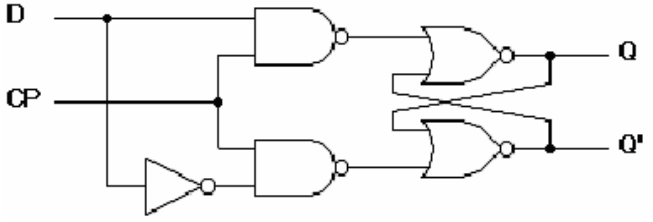

Fig. 14a –*D Flip Flop.*

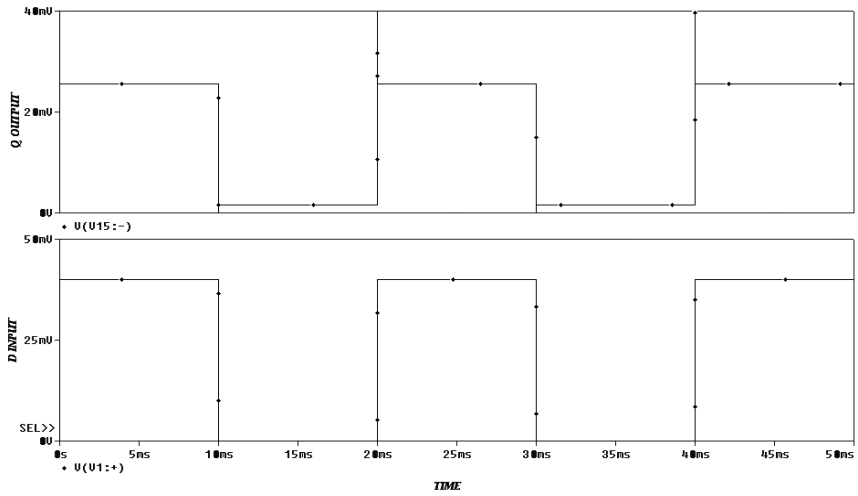

Fig. 14b – *Input and output Response.*

4 Control Logic Using Set Based P-Controller for PWM Signal Generation

The block diagram of buck converter to implement the control scheme is shown in Fig.15. The output of buck converter is forwarded to the comparator for the purpose of its comparison with the reference voltage to produce error signal. This error voltage is proceeded to P-controller [11]. The proportional control offers smoother response to process changes than ON/OFF control. A proportional controller adjusts its control action to the requirements of the process system. The various digital error samples $e(n)$ of converter are given as input to 3 bit shift register. The gain is improved by shifting the pulses to produce output of $d(n) = G_p e(n)$ where G_p is the gain of P controller.

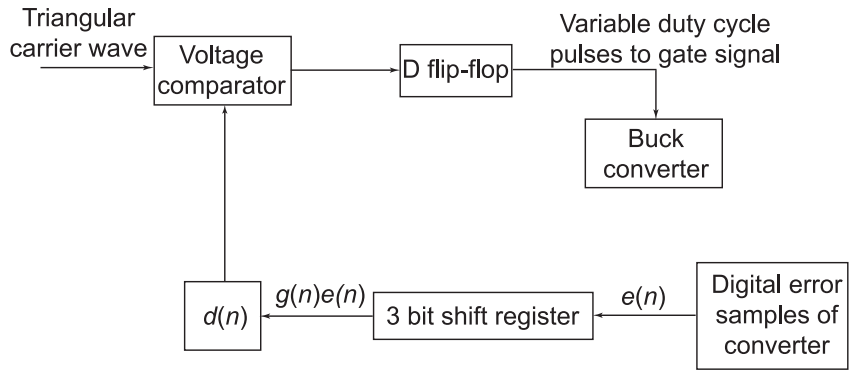

Fig. 15 – *Control Circuit of* PWM *Controller.*

This new duty-cycle output is compared with triangular carrier wave in a voltage comparator, and the comparator output is forwarded to the 'd' latch which provides the production of variable duty cycle pulses that switch the converter circuit. Here SET-based shift register and D latch are implemented whereby the switching speed is greater and the ripple content in the converter output is reduced.

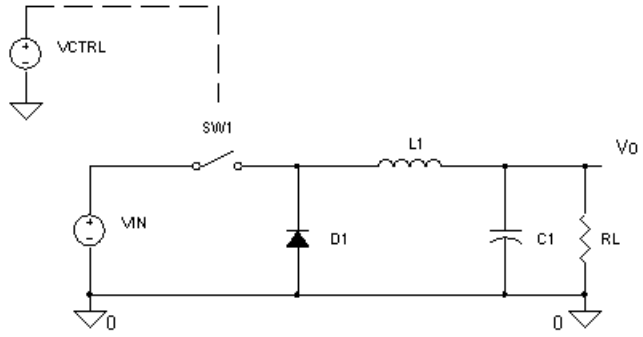

Fig. 16 – *Buck Converter.*

Depending on the output voltage, the pulse width that produces variable duty cycle pulses that turn on the latch is varied. Thus the duty cycle pulses are governed by the produced control signal used as a gating signal that switches the Buck converter circuit. There are only four main components, i.e. switching power MOSFET Q1, flywheel diode D1, inductor L and output filter capacitor C_1. A control circuit monitors the output voltage maintaining it at the desired level by switching Q1 on and off at a fixed rate (the converter's operating frequency), but with a varying duty cycle (the Proportion of each switching period that Q1 is turned on). When Q1 is turned on, current begins flowing from the input source through Q1 and L, and then into C_1 and the load. Therefore the magnetic field in L builds up, storing energy in the inductor with the voltage drop across L opposing or bucking part of the input voltage. Further, when Q1 is turned off, the inductor opposes any drop in current by suddenly reversing its EMF, and subsequently supplies current to the load itself via D1. Without going too deeply into its operation, the DC output voltage appearing across the load is a fraction of the input voltage. This fraction turns out to be equal to the duty cycle. $V_{out}/V_{in} = D$, or $V_{out} = DV_{in}$, where D is the duty cycle, equal to T_{on}/T, where T is the inverse of the operating frequency. Thus by varying the switching duty cycle, the buck Converter's output voltage can be varied as a Fraction of the input voltage [12].

The hierarchical block of 3-Bit Shift register is shown in Fig. 17, the S1, S2 and S3 being the gate signals and f_1, f_2 and f_3 the outputs of the shift register.

Depending on the gate signals, the corresponding SETs are turned ON and the input is connected to the output port. The shifting operation occurs ensuring thus gain improvement.

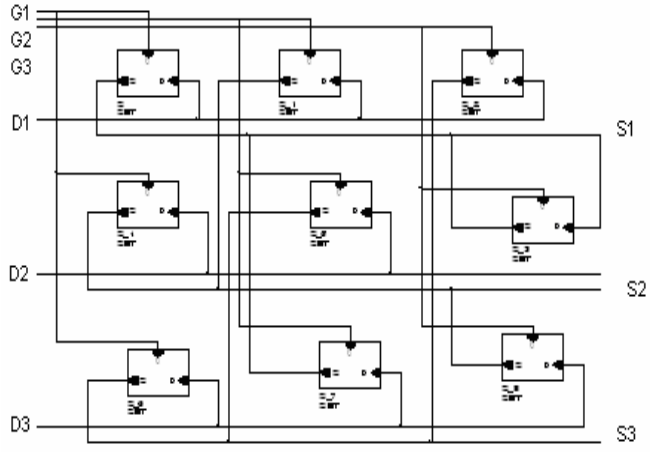

Fig. 17 – 3 Bit *Shift Register.*

Table 1

3-Bit *Shift Register.*

Gate Signals			Inputs			Outputs		
S1	S2	S3	D1	D2	D3	F1	F2	F3
0	0	1	A	B	C	B	C	A
0	1	0	A	B	C	C	A	B
1	0	0	A	B	C	A	B	C

The Logic of the Shift register is tabulated and given in **Table 1**. The Fig. 18 shows the 3-bit shift register output. Here, the gate inputs are 0,1,0 and the inputs are 1,0,1 which is A,B,C ,therefore the output obtained are 1,1,0 which is C,A,B. In Fig .19, the output of Comparator 2 is shown.

The simulation result of control logic to produce PWM pulses is shown in Fig. 20. This is given to switch the converter circuit. Here both open loop and closed loop response of SET-based PWM converter is analyzed.

The Fig. 21 shows the PWM output generated from the SET-based control circuit. This infers that it generates variable duty cycle pulses that switch the converter circuit.

The open loop converters output using SET is shown in Fig. 22. This infers that the output voltage is bucked (reduced) to 4.5V from the input voltage of comparator, i.e. 12V.

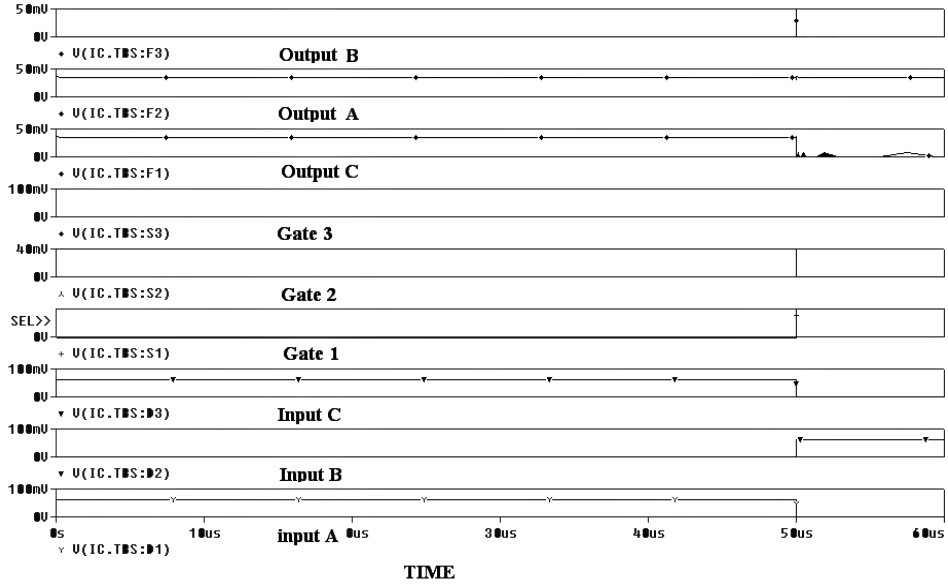

Fig. 18 – 3 Bit *Shift Register Output.*

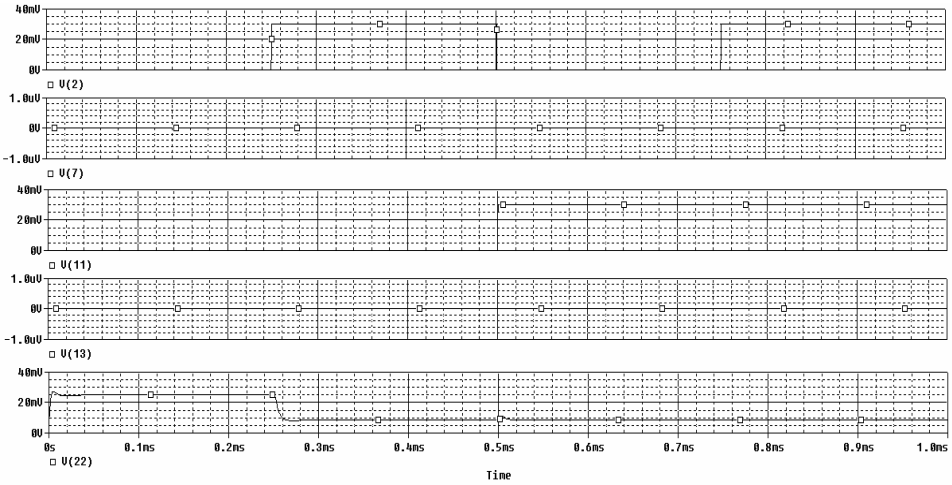

Fig. 19 – *Output of Comparator.*

The Fig. 23 shows the closed loop PWM output using SET-based control circuit. The figure infers that the closed loop produces variable duty cycle pulses that switch the converter circuit. The Fig. 24 shows the closed loop converter output using SET. The following data are inferred from the analysis:

Duty Cycle = 0.54, Desired Voltage = 6.48V, Actual Voltage = 6.45V.

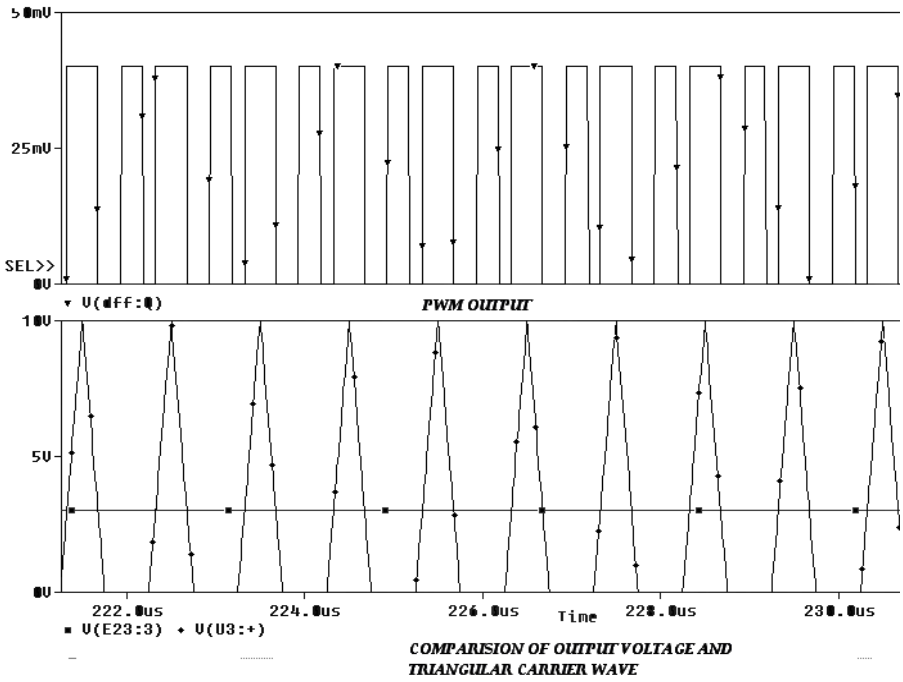

Fig. 20 – *Simulation output.*

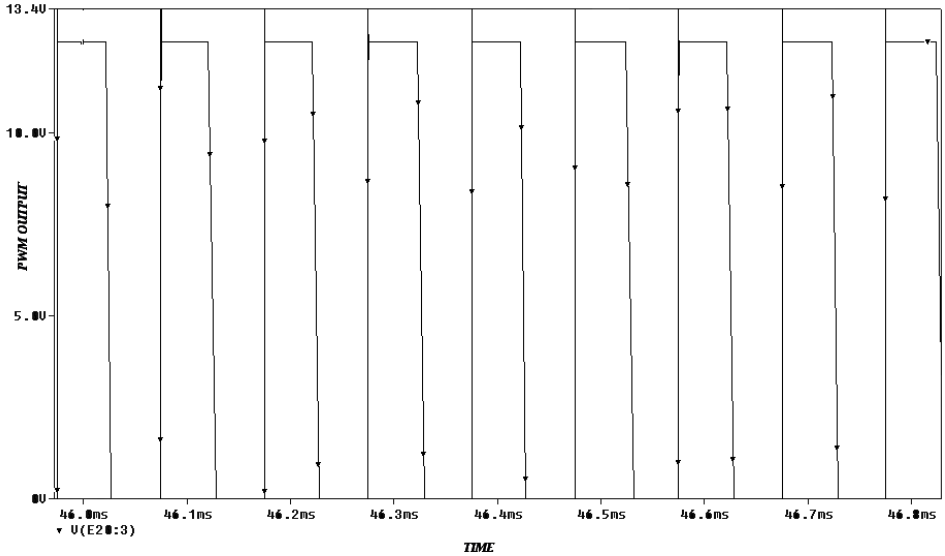

Fig. 21 – *Open Loop* PWM *Output using* SET.

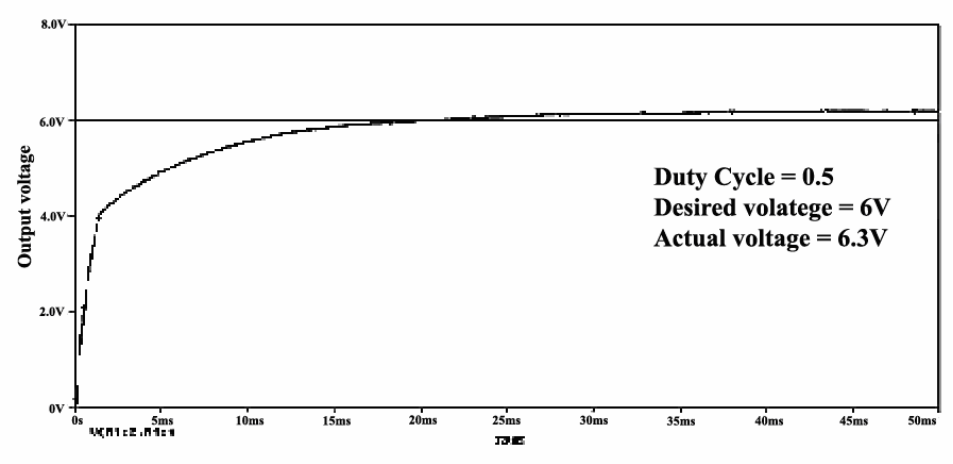

Fig. 22 – *Open Loop Buck Converter Output using* SET.

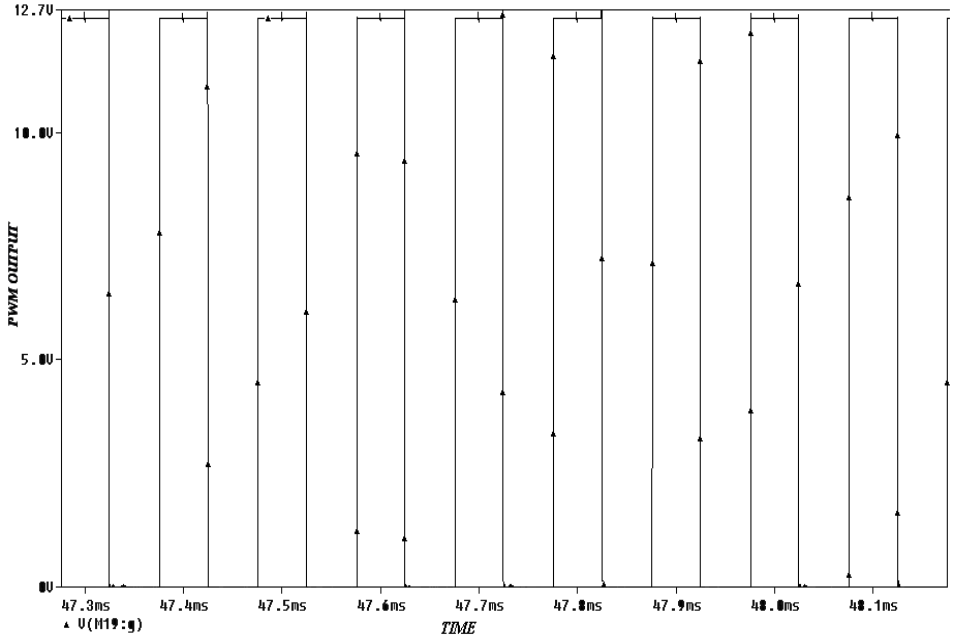

Fig. 23 – *Closed loop* PWM *output.*

The performances of open loop and closed loop SET- and CMOS-based PWM converter are tabulated and shown in **Tables 2** and **3**. In simulation, SET-based circuit is more sensitive in comparison with the one of CMOS. It settles

quicker and attains the desired value in comparison with the latter since the ripple content in the output is lower.

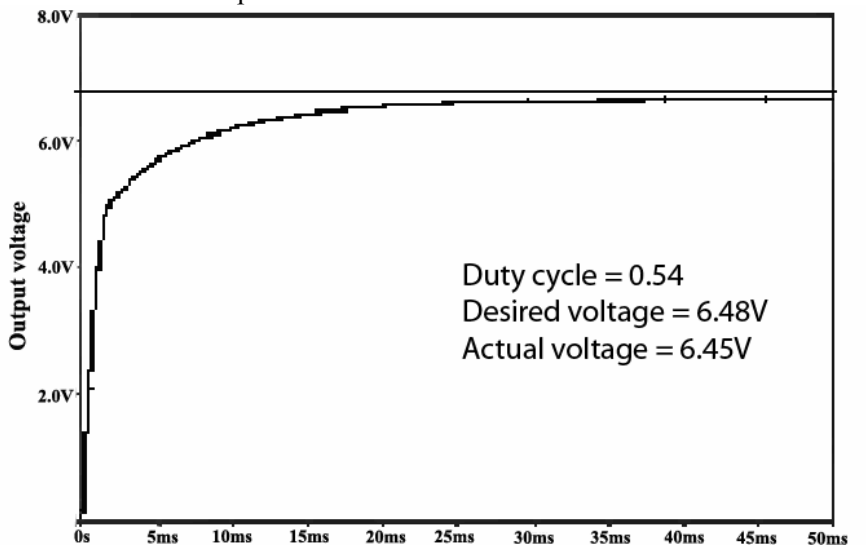

Fig. 24. – *Closed Loop Buck Converter Output using SET*

Table 2

Open loop comparisons of SET *and* CMOS *circuits.*

Duty Cycle		Ref Voltage	On Time		Desired O/p Voltage		Actual O/p Voltage	
CMOS	SET		CMOS	SET	CMOS	SET	CMOS	SET
0.05	0.06	1	0.005	0.006	0.6	0.072	0.9	1.04
0.09	0.09	2	0.009	0.009	1.08	1.08	2	2.10
0.15	0.16	3	0.015	0.016	1.8	1.92	2.88	2.94
0.2	0.2	4	0.02	0.02	2.4	2.4	3.75	3.67
0.25	0.31	5	0.025	0.031	3	3.72	4.38	4.36
0.29	0.32	6	0.029	0.032	3.48	3.84	4.9	4.75
0.34	0.35	7	0.034	0.035	4.08	4.2	5.37	5.30
0.4	0.41	8	0.04	0.041	4.8	4.92	5.72	5.72
0.45	0.46	9	0.045	0.046	5.4	5.52	6.05	6.03

The gate length of SET will be in few nanometers [13, 14] scale hence the fabrication size is smaller as compared to CMOS. In addition, these devices consume less power and are capable of measuring charges with extremely high sensitivity.

Table 3

Closed loop comparisons of SET *and* CMOS *circuits.*

Ref Voltage	On Time		Duty Cycle		Desired O/p Voltage		Actual O/p Voltage	
	CMOS	SET	CMOS	SET	CMOS	SET	CMOS	SET
1	0.031	0.028	0.31	0.28	3.72	3.36	4.94	4.99
2	0.034	0.032	0.34	0.32	4.08	3.84	5.2	5.35
3	0.037	0.042	0.37	0.42	4.44	5.04	5.5	5.56
4	0.040	0.042	0.40	0.42	4.8	5.04	5.81	5.81
5	0.045	0.044	0.45	0.44	5.4	5.28	6.04	6.03
6	0.049	0.049	0.49	0.49	5.8	5.88	6.27	6.27
7	0.053	0.054	0.53	0.54	6.36	6.48	6.4	6.45
8	0.056	0.057	0.56	0.57	6.72	6.48	6.65	6.25
9	0.060	0.061	0.60	0.61	7.2	7.32	6.8	6.79

The total power dissipation in the circuit will be in some nanowatts hence power consumption and heat losses will be reduced. Due to the simplicity and accuracy of compact model the simulation time and speed are faster.

5 Power Dissipation and Dimension

The qualitative and quantitative comparisons of CMOS and SET logic circuits have been discussed in this section. The power estimation, dimension and delay are summarized.

Power consumption:

CMOS:

Total power dissipation $= P_{DC} + P_{DYN}$

$P_{DC} = V_{DD} I_{DD}$

$P_{DYN} = C_{OUT} V_{DD}^2$

Power dissipation = 0.04 W

SET:

Total power dissipation = 1.8 nW

Hence the power consumption of SET circuit is lesser comparing to CMOS circuit and therefore it consumes low power.

Dimension:

CMOS:

Gate Length (L) = 2 μm

Total CMOS used = 18

Total gate length =18 · 2 μm = 36 μm

SET:

Gate Length (L) = 10 nm

Total SET used = 18

Total gate length =18 · 10nm = 180 nm

The gate length of SET circuit is lesser comparing to CMOS circuit and hence Unit size is smaller.

Speed

CMOS:

The speed of CMOS can be estimated in terms of frequency (f)

$$f = P/(C_{out}V_{DD}^2)$$

Power Dissipation: $P = 0.04\,\mathrm{W}$

Supply Voltage: $V_{DD} = 5\,\mathrm{V}$

Output Capacitance: $C_{out} = 1.725\,\mathrm{nF}$

Hence the frequency is 1MHz

SET:

The speed of SET can be estimated by $1/RC$

Resistance: $R = 10^5\,\Omega$

Capacitance: $C = 1.43\,\mathrm{fF}$

Hence the frequency is 6.99 GHz.

Table 4

Comparisons of CMOS *and* SET *based* PWM *controller.*

Parameters	CMOS	SET
Power dissipation	0.04 W	1.8 nW
Dimension (in terms of gate length L)	36 μm	180 nm
Speed	1 MHz	6.99 GHz

It is evident from the analysis and **Table 4** that the Single electron transistor-based PWM controller consumes very little power in the range of nW and could be operated at high speed in the range of a few GHz and over and above the size is very small. Hence this kind of controller can be effectively used for any control action.

6 Conclusion

In this paper a simple SPICE schematic SET model has been proposed and uses. The simulation results clearly indicate that the proposed model provides accurate results. This model has been used in designing SET-based PWM controller. The performance of this controller has been analysed and successfully applied to a buck converter. Finally, the performance measures were compared with that of the CMOS circuits, and it was confirmed that the SET-based PWM controller consumes little power and operates at high speeds without affecting the performance of the converter. Hence in future it is necessary to replace the conventional CMOS devices with advanced nano devices in control circuits so as to improve the overall performance of the converter.

7 References

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